STARTECH

An EXAR Company

ST16C654

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QUAD UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER WITH 64 BYTES OF FIFO AND INFRARED ENCODER/DECODER

DESCRIPTION

The ST16C654 is a Quad universal asynchronous receiver and transmitter with 64 bytes of transmit and receive FIFO. ST16C654 provides dual foot print compatibility with ST16C554 and ST68C554. A programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 1.5 MHz.

The ST16C654 is an improved version of the ST16C554 UART with deeper FIFO, software/ hardware flow control. The ST16C654 on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements. The ST16C654 provides internal loop-back capability for on board diagnostic testing.

The ST16C654 is fabricated in an advanced CMOS process to achieve low drain power and high speed requirements.

FEATURES

- Pin to pin and functional compatible to ST16C454, ST16C554, ST16C554D, ST68C454, ST68C554
- 64 byte transmit FIFO
- 64 byte receive FIFO with error flags
- Software/Hardware flow control
- Programmable Xon/Xoff characters
- Sleep mode (200μA stand-by)
- Low operating current (7mA typ.)
- Independent transmit and receive control
- 460.8 kHz transmit/receive operation
- Selectable Transmit/Receive trigger levels
- Infrared receive and transmit, input / output.
- Independent MIDI interface

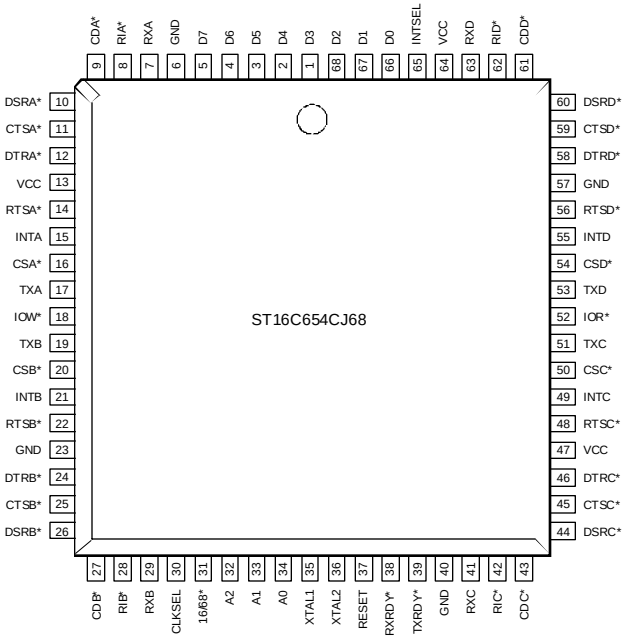
ORDERING INFORMATION

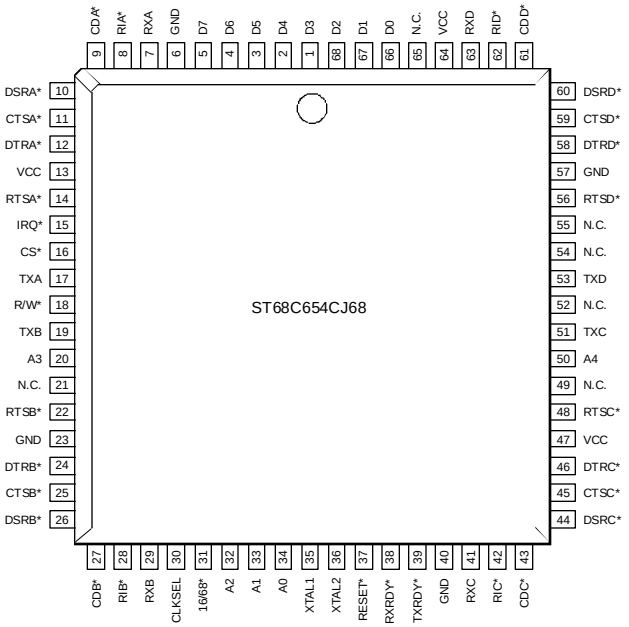
Part number	Package	Operating temperature
ST16C654CJ68	PLCC	0° C to + 70° C
ST16C654CQ64	QFP	0° C to + 70° C
ST16C654DCQ64	QFP	0° C to + 70° C
ST16C654CQ100	QFP	0° C to + 70° C

***Industrial operating range are available**

Rev. 3.2

PLCC Package





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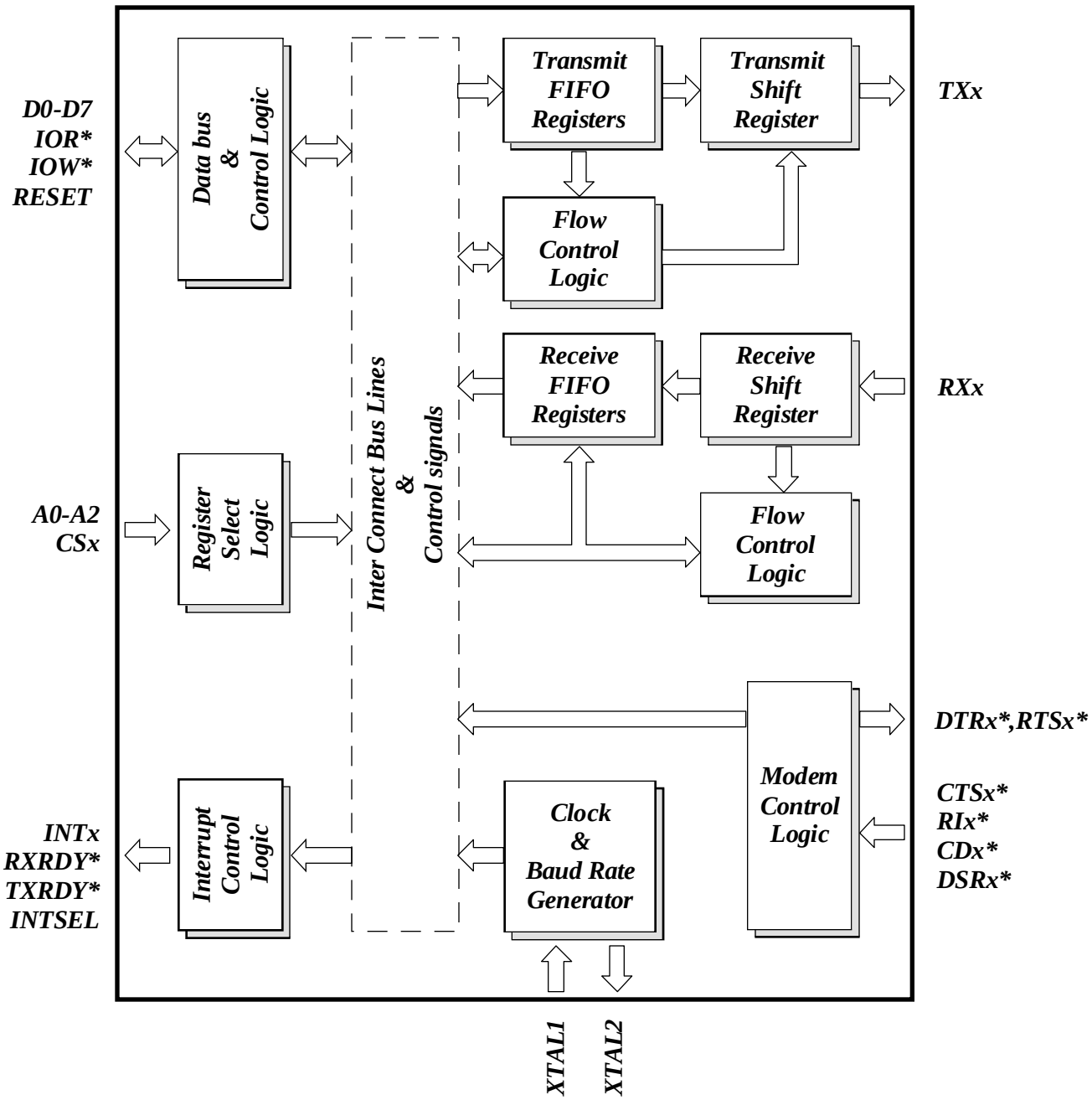
BLOCK DIAGRAM: ST16C654 MODE



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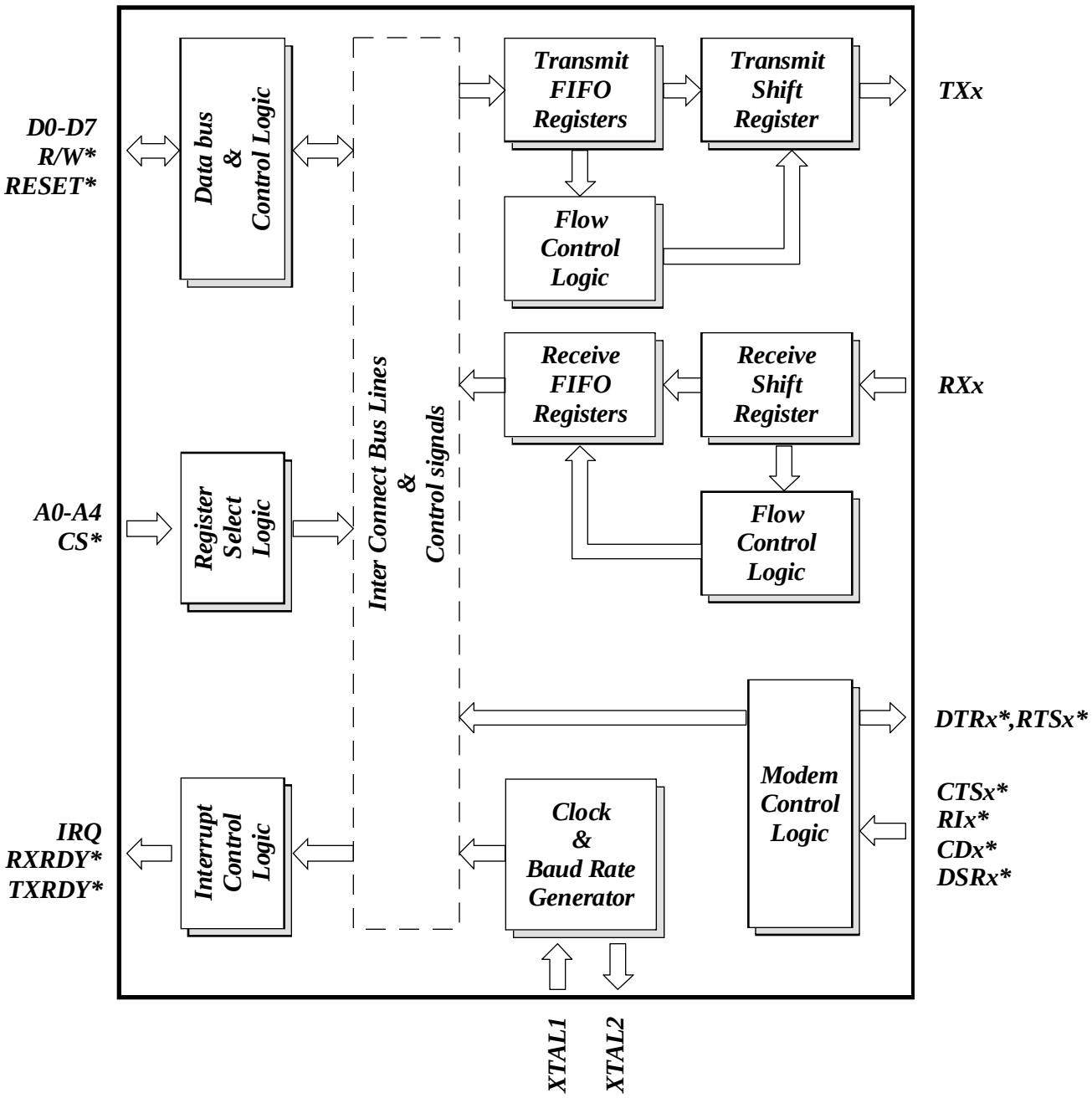
BLOCK DIAGRAM: ST68C654 MODE



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SYMBOL DESCRIPTION

Symbol	Pin 68	Pin 100	Signal Type	Pin Description
D0-D7	66-5	88-95	I/O	Bi-directional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
RX A-B RX C-D	7,29 41,63	97,34 47,85	I	Serial data input (IRRX A-D). The serial information (data) received from serial port to ST16C654 receive input circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
TX A-B TX C-D	17,19 51,53	14,16 65,67	O	Serial data output. The serial data is transmitted via this pin with additional start , stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
IRTX A-B IRTX C-D	- -	6,24 57,75	O	Serial IRda data output. The serial IRda data is transmitted via this pin with additional start , stop and parity bits. The IRTX will be held in mark (low) state during reset.
CS*	16	13	I	Chip select. (active low) This pin functions as chip select when 16/68* pin is connected to GND. All four UARTS will be selected when CS* is low. Each individual UART can be selected with A3-4 combinations. When 16/68* pin is connected to VCC or left open, this pin functions as CSA*.
CS* A-B CS* C-D	16,20 50,54	13,17 64,68	I	Chip select. (active low) A low at this pin enables the ST16C654 / CPU data transfer operation. Each UART sections of the ST16C654 can be accessed independently.
XTAL1	35	40	I	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.

SYMBOL DESCRIPTION

Symbol	Pin 68	Pin 100	Signal Type	Pin Description
XTAL2	36	41	O	Crystal input 2 or buffered clock output. See XTAL1.
MIDICLK	-	42	I	Midi clock input. RXC and TXC can function as midi input / output port when an external midi clock is provided at this pin. MIDICLK can be connected to XTAL2 pin for normal operation.
CLKSEL	30	35	I	Default clock select. 1X or 1X/4 clock can be selected by connecting this pin to VCC or GND. 1X clock is selected when CLKSEL is connected to VCC and 1X/4 is selected when CLKSEL is connected to GND. The MCR bit-7 can override the default clock setup after reset when it is programmed to “1”.
R/W*	18	15	I	Read/Write strobe. This pin acts as Read/Write strobe when 16/68* is connected to GND. A low on this pin will transfer the contents of the CPU data bus to the addressed register. A high on this pin will transfer the contents of the ST16C654 selected register to CPU data bus. When 16/68* pin is connected to VCC or left open, this pin functions as IOW*.
IOW*	18	15	I	Write strobe. (active low) A low on this pin will transfer the contents of the CPU data bus to the addressed register.
GND GND	6,23 40,57	96,20 46,71	O	Signal and power ground.
IOR*	52	66	I	Read strobe. (active low) A low level on this pin transfers the contents of the ST16C654 data bus to the CPU.
TXRDY*	39	45	O	Transmit ready. (active low) TXRDY* pin is the wire “OR-ed” function of all TXRDY* A-D.
TXRDY* A-B TXRDY* C-D	- -	5,25 56,81	O	Transmit ready. (active low) This pin goes when transmit FIFO of the ST16C654 is full. It can be used as a single or multi-transfer.
A3-A4	20,50	17,64	I	Address select line 3 and 4. When 16/68* pin is connected

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SYMBOL DESCRIPTION

Symbol	Pin 68	Pin 100	Signal Type	Pin Description
				to GND, combination of these pins will select individual UART's when CS* is low. When 16/68* is connected to VCC or left open, these pins function as CSB* and CSC*.
A2	32	37	I	Address select line 2. To select internal registers.
A1	33	38	I	Address select line 1. To select internal registers.
A0	34	39	I	Address select line 0. To select internal registers.
RXRDY*	38	44	O	Receive ready. (active low) RXRDY* pin is the wire "OR-ed" function of the all RXRDY* A-D.
RXRDY* A-B RXRDY* C-D	- -	100,31 50,82	O	Receive ready. (active low) This pin goes low when receive FIFO is full. It can be used as a single or multi-transfer.
INTSEL	65®	87®	I	Interrupt type select. Enable /disable the interrupt three state function. Always active interrupt output can be selected by connecting this pin to VCC (MCR bit-3 does not have any effect on the interrupt output). The three state interrupt output is selected when this pin is left open or connected to GND and MCR bit-3 is set to "1". This has no effect when 16/68* pin is connected to GND. **Since this pin is not available in 64 pin QFP package, two versions of 64 pin QFP packages are offered. ST16C654DCQ64 with this pin bonded to VCC and ST16C654CQ64 with this pin bonded to GND.**
CSRDY*	-	76	I	FIFO ready register select. (active low) Content of the FIFORDY register can be read when this pin goes low. D0-D3 corresponds to inverted TXRDY* A-D, and D4-D7 correspond to RXRDY* A-D.
IRQ*	15	12	O	Interrupt output. (active low, open source) This pin goes low (when enabled by the interrupt enable register) when ever any of the four UART's issue interrupt. An external pull-up resistor is required to be connected to this pin. Function of the IRQ* changes to INTA when 16/68* pin is connected to VCC or left open.

SYMBOL DESCRIPTION

Symbol	Pin 68	Pin 100	Signal Type	Pin Description
INT A-B INT C-D	15,21 49,55	12,18 63,69	O	Interrupt output. (active high) This pin goes high (when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty, or modem status condition flag is detected.
RTS* A-B RTS* C-D	14,22 48,56	11,19 62,70	O	Request to send. (active low) To indicate that the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high. Note that this pin does not have any effect on the transmit or receive operation unless hardware flow control is enabled.
DTR* A-B DTR* C-D	12,24 46,58	9,21 60,72	O	Data terminal ready. (active low) To indicate that ST16C654 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low. This pin will be set to high state after writing a "0" to that register or after the reset . Note that this pin does not have any effect on the transmit or receive operation.
RESET* RESET	37	43	I	Master reset. (active high) A high on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time. When 16/68* is connected to GND, RESET functions as RESET*.
CTS* A-B CTS* C-D	11,25 45,59	8,22 59,73	I	Clear to send. (active low) The CTS* signal is a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS* has no effect on the transmit or receive operation unless hardware flow control is enabled
DSR* A-B DSR* C-D	10,26 44,60	7,23 58,74	I	Data set ready. (active low) A low on this pin indicates the MODEM is ready to exchange data with UART. This pin does not have any effect on the transmit or receive operation.

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SYMBOL DESCRIPTION

Symbol	Pin 68	Pin 100	Signal Type	Pin Description
16/68*	31	36	I	Intel or Motorola bus interface select. Functions of the IOR*, IOW*, INT A-D, and CS* A-D are re-assigned with the state of this pin. When this pin is connected to VCC or left open, Intel bus interface is selected. When this pin is connected to GND, IOW* is re-assigned to R/W*, RESET is re-assigned to RESET*, IOR* is not used, and all INT A-D are wired "OR-ed" and used as open source IRQ output. This pin contains internal pull-up resistor.
CD* A-B CD* C-D	9,27 43,61	99,32 49,83	I	Carrier detect. (active low) A low on this pin indicates the carrier has been detected by the modem.
RI* A-B RI* C-D	8,28 42,62	98,33 48,84	I	Ring detect indicator. (active low) A low on this pin indicates the modem has received a ringing signal from telephone line.
VCC VCC	13 47,64	10 61,86	I	Power supply input.

® Has internal pull-down resistor.

DESCRIPTION OF NEW FEATURES

The ST16C654 is designed to upgrade the existing 16C550 market. It provides additional features to reduce the software over-head, external glue logic, operating and stand-by current, and maintain the 16C550 software compatibility with existing software's.

After reset ST16C654 is down-ward compatible with ST16C454 / ST68C454 and ST16C554 / ST68C554 except it provides 64 bytes of data FIFO (when ST16C550 mode is enabled) instead of 16 bytes. All other additional features are available through special function register. The ST16C654 offers the software/ Hardware flow control, sleep mode, selectable transmit trigger levels, and two selectable baud rate generators.

Separate clock input has been provided for MIDI applications. MIDICLK pin can be connected to XTAL2 pin for normal operation or an External MIDI clock oscillator for MIDI application.

Four independent Irda specified outputs are provided (100 QFP package only) for IR applications. These output are provided in parallel with regular asynchronous data output.

A separate FIFO ready register is provided to monitor the TXRDY* and RXRDY* of each individual UART's to reduce the polling time.

ST16C654 offers clock select pin for system / board designers to preset the baud rate table After reset. The CLKSEL pin selects the 1X or 1X/4 clock or internal baud rate generator. When CLKSEL is connected to

the VCC pin the 1X clock is selected. 1X/4 clock is selected when CLKSEL is connected to GND.

FUNCTIONAL DESCRIPTIONS

The 64 bytes data FIFO's are enabled when user writes to the ST16C550/ST16C554 FIFO control register. With standard 16C550 parts, the user can only set receive trigger levels but not transmit trigger level. The ST16C654 provides independent trigger levels for both receiver and transmitter. To be compatible with ST16C550, 1 bytes transmit trigger level is selected after reset. The ST16C654 is designed to work with high speed modems and shared network environments, that requires fast processing time. By increasing number of characters in the FIFO, networking units can handle more data within same time. Example: ST16C550 with 16 bytes of data, 115.2k and 8 bits wide word and one stop bit, will take 1.52 ms to transmit 16 bytes of data. But with 64 bytes of data buffer it will take 6.1 ms. This will gives additional time for the CPU to process other applications and reduce the interrupt servicing time.

The contents of the Xon-1,2 and Xoff 1,2 are reset to "0" and user can write any values desired for software flow controls. Different conditions can be set to detect Xon/Xoff characters or start/stop the transmissions. See the table for all possible conditions. When single Xon/Xoff characters are selected, ST16C654 compares the incoming data with these values and controls the transmission, these characters are not stacked in data buffer or FIFO. When any Xon (MCR bit-5) bit is set, the ST16C654 will resume the operation after receiving any character after recognizing the Xoff character. Note that the ST16C654 will transmit Xon character(s) automatically when Xoff character(s) were send and software flow control function were disabled after wards. Special cases are provided to detect the special character and stack it into the data buffer or FIFO. These conditions are selected via Enhanced Feature Register (EFR bit 0-3).

Hardware flow control can be selected when either or both bits of the EFR bit 6-7 are set to "1". When auto CTS is selected, the ST16C654 will stop the transmission as soon as a complete character is transmitted and CTS input level is high. Transmission is resumed after CTS input changes to low level.

When auto RTS* is selected, output of RTS* pin is "AND-ed" with MCR bit-1 for manual over ride capability. RTS* pin will change state when MCR bit-1 is set to "1". RTS* pin will be forced to high state when receive FIFO reaches to the programmed trigger level. RTS* pin resumes it original state after content of the data buffer (FIFO) drops below the next lower trigger level. Both hardware and software flow controls can be enabled for automatic operation. During these conditions the ST16C654 will accept additional data to fill the unused transmit and receive FIFO locations.

Special interrupt modes have been added to monitor the hardware and software flow conditions. These are the IER bits 5-7.

The ST16C654 is designed to operate with low power consumption, special sleep mode has been added to stop the clock and reduce the power consumption when it is not used (Green PC). When EFR bit-4 and IER bit-4 are enabled (set to "1"), the ST16C654 enters into sleep mode and resumes it's normal operation when a data is received or state of the modem input pins changes or it is set to transmit data. The ST16C654 stays in this mode till it is disabled.

Special care should be considered for the following interrupt conditions and handling them. After reset if transmitter interrupt is enabled, ST16C654 will issue an interrupt to indicate that transmit holding register is empty, no other interrupts will be issued after enabling the interrupt. The LSR register has highest interrupt priority and CTS, RTS* have lowest interrupt priority. The interrupt status register will show the highest interrupt priority condition, and after servicing the interrupt condition next priority interrupt level will be shown. There are two interrupt conditions that have same priority and it is important to know the conditions to service. Receive data ready and receive time out share the same priority with one additional bit (IER bit-3). Receiver issues interrupt after number of characters are reached the programmed trigger level, in this case the ST16C654 FIFO holds equal or more characters than the trigger level. After reading block of data, user can check the LSR bit-0 for additional characters.

Note that, receive time out is functional only in

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ST16C550/650 mode. Receive time out will not occur if the receive FIFO is empty. The time out counter will be reset at the center of each stop bit received or each time receive holding register is read. The actual time out value is T (**T**ime out length in bits)= 4 X P (**P**rogrammed word length) + 12. To convert time out value to a character value, user has to divide this number to its complete word length + parity (if used) + number of stop bits and start bit.

Example -A: If user programs the word length = 7, and no parity and one stop bit, Time out will be:
T = 4 X 7(programmed word length) +12 = 40 bits
Character time = 40 / 9 [(programmed word length = 7) + (stop bit = 1) + (start bit = 1)] = 4.4 characters.

Example -B: If user programs the word length = 7, with parity and one stop bit, the time out will be:
T = 4 X 7(programmed word length) + 12 = 40 bits
Character time = 40 / 10 [(programmed word length = 7) + (parity = 1) + (stop bit = 1) + (start bit = 1) = 4 characters.

Dual baud rate generator is provided to maintain the 16C550 compatibility and provide higher data rate when it is needed. Example 14.4k to 19.2k modems requires to have 57k to 115.2k data rate and 28.8k modem requiems to have 230.4K. The 16C550 compatible parts can only offer 115.2k to maintain the software compatibility. The ST16C654 utilizes 7.32 MHz crystal/clock and provide 16C550 compatible data rate and higher. ST16C550 and ST16C654 baud rate generator tables can be selected is setting and resetting the MCR bit-7. After hardware reset the ST16C654 will set the baud rate table according to pin state of the CLKSEL.

The ST16C654 transmit trigger level, provides additional flexibility to the user for block mode operation. In ST16C550/650 mode LSR bits 5-6 gives indication that transmitter is empty or not, but there is no mechanism to identify FIFO full state or available empty locations in FIFO. User can select one of the two possible ways to operate the transmit and receive FIFO by utilizing the DMA mode (FCR bit-3). When FIFO's are enabled and DMA mode "0" is selected, the ST16C654 sets the interrupt bit and activates interrupt output pin for single transmit and receive operation like ST16C450 mode except it can receive and transmit 64 bytes of characters. When DMA mode "1" is activated, user takes the advantage of the block mode operation. In this mode, transmitter/receiver sets the interrupt flag and interrupt output pin, when characters in the FIFO are below the transmit trigger level or over receive trigger level. Note that since ST16C550 does not have transmit trigger levels, the default trigger level in the ST16C654 is set to 1 byte (trigger level "0").

SERIAL PORT SELECTION GUIDE

CS*	A4	A3	UART X
1	x	x	x
0	0	0	UART A
0	0	1	UART B
0	1	0	UART C
0	1	1	UART D

This table is valid when 16/68* pin is connected to GND. Otherwise each UART is selected with individual CSx pins.

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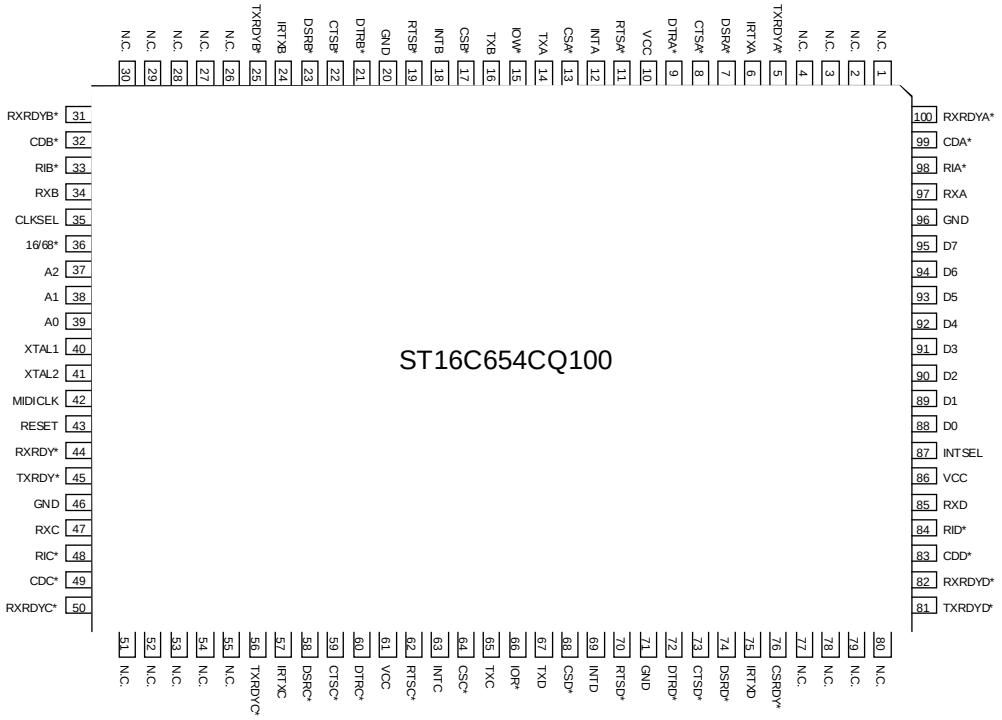
PROGRAMMING TABLE

A2	A1	A0	READ MODE	WRITE MODE
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1		Interrupt Enable Register
0	1	0	Interrupt Status Register	FIFO Control Register
0	1	1		Line Control Register
1	0	0		Modem Control Register
1	0	1	Line Status Register	
1	1	0	Modem Status Register	
1	1	1	Scratchpad Register	Scratchpad Register
0	***0***	***0***	***LSB of Divisor Latch***	***LSB of Divisor Latch***
0	***0***	***1***	***MSB of Divisor Latch***	***MSB of Divisor Latch***
0	***1***	***0***	***Enhanced Feature Register***	***Enhanced Feature Register***
1	***0***	***0***	***Xon-1 Word***	***Xon-1 Word***
1	***0***	***1***	***Xon-2 Word***	***Xon-2 Word***
1	***1***	***0***	***Xoff-1 Word***	***Xoff-1 Word***
1	***1***	***1***	***Xoff-2 Word***	***Xoff-2 Word***

These registers are accessible only when LCR bit-7 is set to "1". Enhanced Feature Register, Xon1,2 and Xoff1,2 are accessible only when LCR is set to "BF"



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ST16C654 ACCESSIBLE REGISTERS

A2	A1	A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0	0	0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	1	IER	0/ CTS interrupt	0/ RTS* interrupt	0/ Xoff interrupt	0/ Sleep mode	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0	1	0	FCR	RCVR trigger (MSB)	RCVR trigger (LSB)	0/TX trigger (MSB)	0/TX trigger (LSB)	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFO enable
0	1	0	ISR	0/ FIFO's enabled	0/ FIFO's enabled	0/ RTS*, CTS	0/ Xoff	int priority bit-2	int priority bit-1	int priority bit-0	int status
0	1	1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1	0	0	MCR	Clock select	0/ IRRT enable	0/ Xon Any	loop back	OP2*/ IRQx enable	OP1*/ no output	RTS*	DTR*
1	0	1	LSR	0/ FIFO error	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1	1	0	MSR	CD	RI	DST	CTS	delta CD*	delta RI*	delta DSR*	delta CTS*
1	1	1	SPREE	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	***0***	***0***	***DLL***	***bit-7***	***bit-6***	***bit-5***	***bit-4***	***bit-3***	***bit-2***	***bit-1***	***bit-0***
0	***0***	***1***	***DLL***	***bit-15***	***bit-14***	***bit-13***	***bit-12***	***bit-11***	***bit-10***	***bit-9***	***bit-8***
0	***1***	***0***	***EFR***	***Auto CTS***	***Auto RTS****	***Special Char. select***	***Enable IER Bits 4-7, ISR, FCR Bits 4-5, MCR Bits 5-7***	***Cont-3 Tx,Rx Control***	***Cont-2 Tx,Rx Control***	***Cont-1 Tx,Rx Control***	***Cont-0 Tx,Rx Control***
X	X	X	FIFORdy	RxRdy D	RxRdy C	RxRdy B	RxRdy A	TxRdy D	TxRdy C	TxRdy B	TxRdy A

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REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register (LSR). Writing to this register (THR) will transfer the contents of data bus (D7-D0) to the Transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set.
On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX input. Receiver status codes will be posted in the Line Status Register.

FIFO INTERRUPT MODE OPERATION

When the receive FIFO (FCR BIT-0=1) and receive interrupts (IER BIT-0=1) are enabled, receiver interrupt will occur as follows:

A) The receive data available interrupts will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.

B) The ISR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt it is cleared when the FIFO drops below the trigger level.

C) The data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receiver FIFO. It is reset when the FIFO is empty.

FIFO POLLED MODE OPERATION

When FCR BIT-0=1 puts the ST16C654 in the FIFO polled mode of operation. Since the receiver and transmitter are controlled separately either one or both can be in the polled mode operation by utilizing the Line Status Register.

A) LSR BIT-0 will be set as long as there is one byte in the receive FIFO.

B) LSR BIT4-1 will specify which error(s) has occurred.

C) LSR BIT-5 will indicate when the transmit FIFO is empty.

D) LSR BIT-6 will indicate when both transmit FIFO and transmit shift register are empty.

E) LSR BIT-7 will indicate when there are any errors in the receive FIFO.

PROGRAMMABLE BAUD RATE GENERATOR

The ST16C654 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-24 MHz and dividing it by any divisor from 1 to 2^{16} -1. Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

Patent pending

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BAUD RATE GENERATOR PROGRAMMING TABLE (7.372 MHz CLOCK):

BAUD RATE MCR BIT-7=1	BAUD RATE MCR Bit-7=0	16 x CLOCK DIVISOR "Decimal"
50	200	2304
75	300	1536
150	600	768
300	1200	384
600	2400	192
1200	4800	96
2400	9600	48
4800	19.2K	24
7200	28.8K	16
9600	38.4k	12
19.2K	76.8k	6
38.4K	153.6k	3
57.6K	230.4k	2
115.2K	460.8k	1

HARDWARE FLOW CONTROL OPERATION.

When hardware flow control operation is enabled, the ST16C654 monitors the CTS* pin for transmit operation and receiver trigger level for RTS* operation. When CTS* changes state from low to high, the ST16C654 suspends the transmission operation as soon as complete character is transmitted. ISR bit-5 will be set (if enabled via IER bit 6-7). Transmission will resume as soon as CTS* pin goes low. RTS* pin will be forced to high state when receiver FIFO reached to the programmed trigger level. RTS* will go low when Receive Holding Register is below next lower trigger level. The ST16C654 will accept additional data when transmission is suspended during hardware flow control till all locations are filled.

Auto RTS* is functional only when the MCR bit-1 is set to "1". The RST* output pin can change state by setting MCR bit-1 to "0" or "1". This provides additional flexibility for manual over ride and maintain the hardware flow control functionality.

SOFTWARE FLOW CONTROL

When software flow control operation is enabled, the ST16C654 will compare the two sequential receive data with Xoff-1,2 programmed characters. When these characters matched correctly, the ST16C654 will halt the transmission after finishing the transmission of the complete character. The receive ready, Xoff (if enabled via IER bit-5) flags will be set and the interrupt output pin (if receive interrupt is enabled) will be activated. After the recognition of the Xoff characters the ST16C654 will compare next two incoming characters with Xon-1,2 characters. The ST16C654 will resume the operation and clear the flags (ISR bit-4) when Xon characters are received. The ST16C654 will send Xoff-1,2 characters as soon as received data passed the programmed trigger level. The ST16C654 will transmit programmed Xon-1,2 characters as soon as receive data reached to the next lower trigger level.

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT output pin.

IER BIT-0:
0= disable the receiver ready interrupt.
1=enable the receiver ready interrupt.

IER BIT-1:
0= disable the transmitter empty interrupt.
1= enable the transmitter empty interrupt.

IER BIT-2:
0= disable the receiver line status interrupt.
1= enable the receiver line status interrupt.

IER BIT-3:
0= disable the modem status register interrupt.
1= enable the modem status register interrupt.

IER BIT -4:
0= disable sleep mode.
1= enable sleep mode. The ST16C654 enters into power down mode and external clock or oscillator circuit is disabled. Any change of state on the RX, RI*, CTS*, DSR*, and CD* pins start the ST16C654. The

ST16C654 will not lose the programmed bits when sleep mode is activated or deactivated. The ST16C654 will not enter in sleep mode if any interrupt is pending.

IER BIT-5:
0= disable the received Xoff interrupt.
1= enable the received Xoff interrupt. The ST16C654 issues an interrupt when Xoff characters are received and correctly matched with Xoff 1,2 words.

IER BIT-6:
0= disable the RTS* interrupt.
1= enable the RTS* interrupt. The ST16C654 issues interrupt when RTS* pin changes state from low to high.

IER BIT-7:
0= disable the CTS interrupt.
1= enable the CTS interrupt. The ST16C654 issues interrupt when CTS pin changes state from low to high.

INTERRUPT STATUS REGISTER (ISR)

The ST16C654 provides six level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the ST16C654 provides the highest interrupt level to be serviced by CPU. No other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

Priority level

P	D5	D4	D3	D2	D1	D0	Source of the interrupt
1	0	0	0	1	1	0	LSR (Receiver Line Status Register)
2	0	0	0	1	0	0	RXRDY* (Received Data Ready)
2	0	0	1	1	0	0	RXRDY* (Receive Data time out)
3	0	0	0	0	1	0	TXRDY (Transmitter Holding Register Empty)
4	0	0	0	0	0	0	MSR (Modem Status Register)
5	0	1	0	0	0	0	RXRDY* (Received Xoff signal)/ Special character
6	1	0	0	0	0	0	CTS, RTS* change of state

ISR BIT-0:
0= an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
1= no interrupt pending.

ISR BIT 1-3:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 4-5:
These bits are enabled when EFR bit-4 is set to “1”. ISR bit-4 indicates that matching Xoff characters have been detected. ISR bit-5 indicates that CTS, RTS* have been received or issued. Note that the ISR bit-4 will stay “1” till Xon characters are received.

ISR BIT 6-7:
These bits are not used and are set to zero in ST16C450 mode. **BIT 6-7:** are set to “1” in ST16C654 mode.

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FIFO CONTROL REGISTER (FCR)

This register is used to enable the FIFOs, clear the FIFOs, set the receiver FIFO trigger level, and select the type of DMA signaling.

FCR BIT-0:
0= disable the transmit and receive FIFO.
1= enable the transmit and receive FIFO.
This bit should be enabled before setting the FIFO trigger levels.

FCR BIT-1:
0= No change.
1= Clears the contents of the receive FIFO and resets its counter logic to 0 (the receive shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-2:
0= No change.
1= Clears the contents of the transmit FIFO and resets its counter logic to 0 (the transmit shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-3:
0= No change.
1= Changes RXRDY* and TXRDY pins from mode "0" to mode "1".

Transmit operation in mode "0":
When ST16C654 is in ST16C450 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) when there are no characters in the transmit FIFO or transmit holding register, the TXRDY* pin will go low. Once active the TXRDY* pin will go high (inactive) after the first character is loaded into the transmit holding register.

Receive operation in mode "0":
When ST16C654 is in ST16C450 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) and there is at least 1 character in the receive FIFO, the RXRDY* pin will go low. Once active the RXRDY* pin will go high (inactive) when there are no more characters in the receiver.

Transmit operation in mode "1":
When ST16C654 is in FIFO mode (FCR bit-0=1, FCR bit-3=1) the TXRDY* pin will become high (inactive) when the transmit FIFO is completely full. It will be low if one or more FIFO locations are empty.

Receive operation in mode "1":
When ST16C654 is in FIFO mode (FCR bit-0=1, FCR bit-3=1) and the trigger level has been reached, the RXRDY* pin will go low. Once it is activated it will go high (inactive) when there are no more characters in the FIFO.

FCR BIT 4-5:
These bits are used to set the trigger level for the transmit FIFO interrupt. The ST16C654 will issue a transmit empty interrupt when number of characters in FIFO drops below the selected trigger level.

BIT-5	BIT-4	FIFO trigger level
0	0	8
0	1	16
1	0	32
1	1	56

FCR BIT 6-7:
These bits are used to set the trigger level for the receiver FIFO interrupt.

BIT-7	BIT-6	FIFO trigger level
0	0	8
0	1	16
1	0	56
1	1	60

LINE CONTROL REGISTER (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Word length
0	0	5
0	1	6
1	0	7
1	1	8

LCR BIT-2:
The number of stop bits can be specified by this bit.

BIT-2	Word length	Stop bit(s)
0	5,6,7,8	1
1	5	1-1/2
1	6,7,8	2

LCR BIT-3:
Parity or no parity can be selected via this bit.
0= no parity
1=a parity bit is generated during the transmission, receiver also checks for received parity.

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0= ODD parity is generated by forcing an odd number of 1's in the transmitted data, receiver also checks for same format.
1= EVEN parity bit is generated by forcing an even the number of 1's in the transmitted data, receiver also checks for same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.
LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:
Break control bit. It causes a break condition to be transmitted (the TX is forced to low state).
0= normal operating condition.
1= forces the transmitter output (TX) to go low to alert the communication terminal.

LCR BIT-7:
The internal baud rate counter latch and Enhance Feature mode enable (DLAB).
0= normal operation.
1= Divisor latch and Enhanced Feature register enable.

MODEM CONTROL REGISTER (MCR)

This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0= force DTR* output to high.
1= force DTR* output to low.

MCR BIT-1:
0= force RTS* output to high.
1= force RTS* output to low.
RTS* is used as hardware flow control signal when enabled via EFR bit-6. RTS* goes high when FIFO is reached to the selected trigger level and goes low as soon as content of the receive holding register is below the trigger level. Content of this register changes with state of the hardware flow control. functions normally when hardware flow control is disabled.

MCR BIT-2:
This bit is used in internal loop-back mode only.
0= set OP1* output to high.
1= set OP1* output to low.

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MCR BIT-3:
0= set OP2* output to high (internal loopback mode). Forces INTx outputs to three state mode if INTSEL pin is left open or connected to GND. It has no effect if INTSEL pin is connected to VCC.
1= set OP2* output to low (internal loopback mode). Sets the INTx outputs to active mode if INTSEL pin is left open or connected to GND. It has no effect if INTSEL pin is connected to VCC.

MCR BIT-4:
0= normal operating mode.
1= enable local loop-back mode (diagnostics). The transmitter output (TX) is set high (Mark condition), the receiver input (RX) , CTS*, DSR*, CD*, and RI* are disabled. Internally the transmitter output is connected to the receiver input and DTR*, RTS*, OP1* and OP2* are connected to modem control inputs.
In this mode , the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER .

MCR BIT-5:
0 = Disable Xon any function, ST16C550 compatible.
1= Enable Xon any function.

MCR BIT-6:
0= Standard UART receive and transmit input / output.
1= Infrared receive and transmit input / output. The TX A-D outputs and RX A-D inputs are converted to Infrared encoder/decoder output/input format. TX output goes low when this bit is set to “1”.

MCR BIT-7:
0= Normal or divide by one clock input. Standard ST16C550 baud rates can be selected when this bit is set to “0” and 1.8432 MHz crystal is used.
1= Divide by four clock input. Standard ST16C550 baud rates can be selected when this bit is set to “1” and 7.372 MHz crystal is used.

LINE STATUS REGISTER (LSR)

This register provides the status of data transfer to CPU.

LSR BIT-0:
0= no data in receive holding register or FIFO.
1= data has been received and saved in the receive holding register or FIFO.

LSR BIT-1:
0= no overrun error (normal).
1= overrun error, next character arrived before receive holding register was emptied or if FIFOs are enabled, an overrun error will occur only after the FIFO is full and the next character has been completely received in the shift register. Note that character in the shift register is overwritten, but it is not transferred to the FIFO.

LSR BIT-2:
0= no parity error (normal).
1= parity error, received data does not have correct parity information. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-3:
0= no framing error (normal).
1= framing error received, received data did not have a valid stop bit. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-4:
0= no break condition (normal).
1= receiver received a break signal (RX was low for one character time frame). In FIFO mode, only one zero character is loaded into the FIFO.

LSR BIT-5:
It indicates that the ST16C654 is ready to accept a new character for transmission. In addition, it causes the ST16C654 to issue an interrupt to the CPU when the transmit holding register empty interrupt enable is set.

0= transmit holding register is not empty.
1= transmit holding register (or FIFO) is empty. CPU can load the next characters. When this bit is set, CPU can load upto 64 bytes of data to the ST16C654.

LSR BIT-6:
0= transmitter holding and shift registers are full.
1= transmitter holding and shift registers are empty. In FIFO mode this bit is set to one whenever the transmitter FIFO and transmit shift register are empty.

LSR BIT-7:
0= normal.
1= at least one parity error, framing error or break indication in the FIFO. This bit is cleared when LSR is read.

MODEM STATUS REGISTER (MSR)

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:
Indicates that the CTS* input to the ST16C654 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR* input to the ST16C654 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI* input to the ST16C654 has changed from a low to a high state.

MSR BIT-3:
Indicates that the CD* input to the ST16C654 has changed state since the last time it was read.

MSR BIT-4:
This bit is equivalent to RTS* in the MCR during local loop-back mode. It is the compliment of the CTS* input.
CTS* functions as hardware flow control signal input if it is enabled via EFR bit-7. Transmit holding register is gated with this input to start/stop the transmission. A high at this pin will stop the transmission as soon as complete character is transmitted.

MSR BIT-5:
This bit is equivalent to DTR in the MCR during local loop-back mode. It is the compliment of the DSR* input.

MSR BIT-6:
This bit is equivalent to OP1 in the MCR during local loop-back mode. It is the compliment of the RI* input.

MSR BIT-7:
This bit is equivalent to OP2 in the MCR during local loop-back mode. It is the compliment to the CD* input.

Note: Whenever MSR BIT3-0: is set to logic "1", a MODEM Status Interrupt is generated.

SCRATCHPAD REGISTER (SR)

ST16C654 provides a temporary data register to store 8 bits of information for variable use.

ENHANCED FEATURE REGISTER (EFR)

Enhanced Features can be Enable/Disabled via this register.

EFR BIT 0-3:
Combinations of software flow control can be selected by programming this bits.

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Cont-3	Cont-2	Cont-1	Cont-0	Tx, Rx software flow controls
0	0	X	X	No transmit flow control
1	0	X	X	Transmit Xon1, Xoff1
0	1	X	X	Transmit Xon2, Xoff2
1	1	X	X	Transmit Xon1 and Xon2 : Xoff1, Xoff2
X	X	0	0	No receive flow control
X	X	1	0	Receiver compares Xon1, Xoff1
X	X	0	1	Receiver compares Xon2, Xoff2
1	0	1	1	Transmit Xon1, Xoff1. Receiver compares Xon1 or Xon2, Xoff1 or Xoff2
0	1	1	1	Transmit Xon2, Xoff2 Receiver compares Xon1 or Xon2, Xoff1 or Xoff2
1	1	1	1	Transmit Xon1 and Xon2 : Xoff1 and Xoff2 Receiver compares Xon1 and Xon2 : Xoff1 and Xoff2
0	0	1	1	No transmit flow control Receiver compares Xon1 and Xon2 : Xoff1 and Xoff2

EFR BIT-4:
Enhanced functions enable bit.
0= disables the IER bits 4-7, ISR bits 4-5, FCR bits 4-5 and MCR bits 5-7. After hardware reset, the IER bits 4-7, ISR bits 4-5, FCR bits 4-5, and MCR bits 5-7 are set to “0” to be compatible with ST16C550 mode.
1= enables the enhanced functions. When this bit is set to “1” all enhanced features of the ST16C654 are enabled. The content of the IER bits 4-7, ISR bits 4-5, FCR bits 4-5, and MCR bits 5-7 can be modified and latched. After modifying the IER bits 4-7, ISR bits 4-5, FCR bits 4-5, and MCR bits 5-7, the EFR bit-4 can be set to “0” to latch the contents of the new values, this feature is provided to prevents the existing software’s to alter / overwrite the ST16C654 enhanced functions.

EFR BIT-5:
0= Normal.
1= Special character detect. ST16C654 compares the incoming receive data with Xoff-2 data. Up on correct match, the received data will be transferred to FIFO and ISR Bit-4 will be set to indicate detection of special character.

EFR BIT-6:
RTS* flow control.
0 = Normal. RTS* flow control is disabled. Standard ST16C550 mode.
1 = RTS* pin goes high when receive FIFO’s are reach to the programmed trigger level.

EFR Bit-7:
CTS* flow control.
0 = Normal. CTS* flow control mode is disabled. Standard ST16C550 mode.
1 = Transmission is resumed when low input signal is detected on the CTS* pin.

FIFO READY REGISTER

This register provides the state of the transmit and receive FIFO.

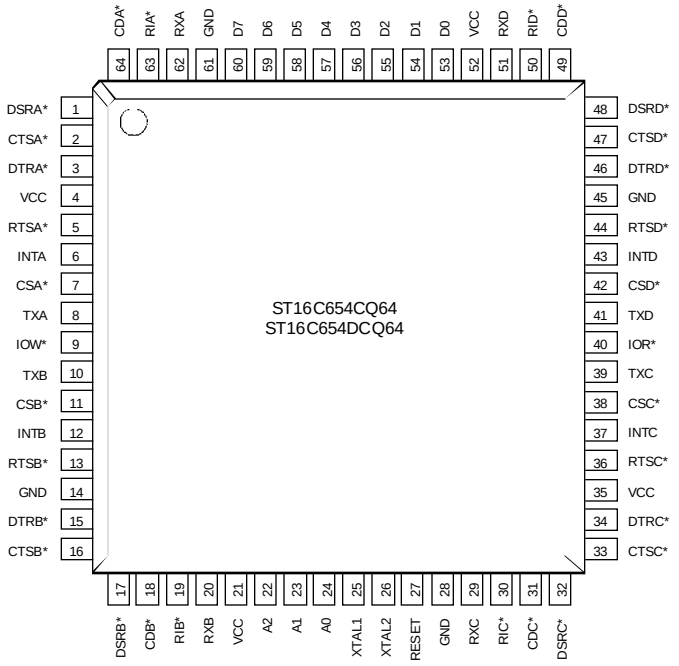
FIFORdy Bit 0-3:
0 = Transmit FIFO is full. The ST16C650 can not take any more transmit data.
1 = One or more empty location in FIFO or FIFO is below transmit trigger level.

FIFORdy Bit 4-7:
0 = Receiver is above the trigger level or timeout is occurred.
1 = Receiver is not ready.

SIGNALS	RESET STATE
TX A-D	High
RTS* A-D	High
DTR* A-D	High
RXRDY* A-D	High
TXRDY* A-D	Low

ST16C654 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE
IER	IER BITS 0-7=0
ISR	ISR BIT-0=1, ISR BITS 1-7=0
LCR	LCR BITS 0-7=0
MCR	MCR BITS 0-7=0
LSR	LSR BITS 0-4=0, LSR BITS 5-6=1 LSR, BIT 7=0
MSR	MSR BITS 0-3=0, MSR BITS 4-7= input signals
FCR	FCR BITS 0-7=0
EFR	EFR BITS 0-7=0



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AC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C (-40° - +85° C for IJ,IQ packages), Vcc=3.3 - 5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits			Units	Conditions
		Min	Typ	Max		
T_1	Clock high pulse duration	20			ns	
T_2	Clock low pulse duration	20			ns	
T_8	Chip select setup time	0			ns	
T_9	Chip select hold time	0			ns	
T_{12}	Data setup time	15			ns	
T_{13}	Data hold time	15			ns	
T_{14}	IOW* delay from chip select	0			ns	
T_{15}	IOW* strobe width	40			ns	
T_{16}	Chip select hold time from IOW*	0			ns	
T_{17}	Write cycle delay	40			ns	
T_{18}	Data valid delay time			15	ns	
Tw	Write cycle=T_{15}+T_{17}	80			ns	
T_{19}	Data hold time	10		15	ns	
T_{21}	IOR* delay from chip select	10			ns	
T_{23}	IOR* strobe width	40			ns	
T_{24}	Chip select hold time from IOR*	0			ns	
T_{25}	Read cycle delay	40			ns	
Tr	Read cycle=T_{23}+T_{25}	80			ns	
T_{26}	Delay from IOR* to data			20	ns	100 pF load
T_{28}	Delay from IOW* to output			35	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM			70	ns	100 pF load
T_{30}	Delay to reset interrupt from IOR* input			70	ns	100 pF load
T_{31}	Delay from stop to set interrupt			1_{RClk}		100 pF load
T_{32}	Delay from IOR* to reset interrupt			200	ns	100 pF load
T_{33}	Delay from initial INT reset to transmit start	8		24	*	
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from IOW* to reset interrupt			175	ns	
T_{44}	Delay from stop to set RxRdy			1_{RCLK}		
T_{45}	Delay from IOR* to reset RxRdy			100	ns	
T_{46}	Delay from IOW* to set TxRdy			195	ns	
T_{47}	Delay from start to reset TxRdy			8	*	
T_R	Reset pulse width	10			ns	

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ABSOLUTE MAXIMUM RATINGS

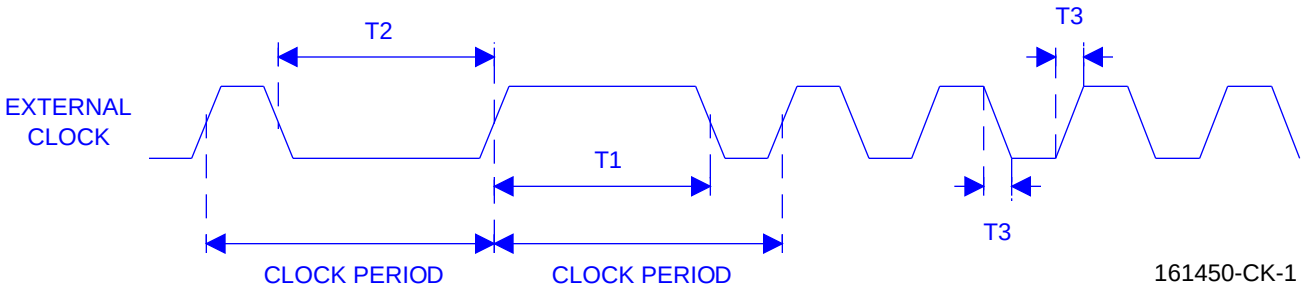
Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C (-40° - +85° C for IJ,IQ packages), Vcc=3.3 - 5.0 V ± 10% unless otherwise specified.

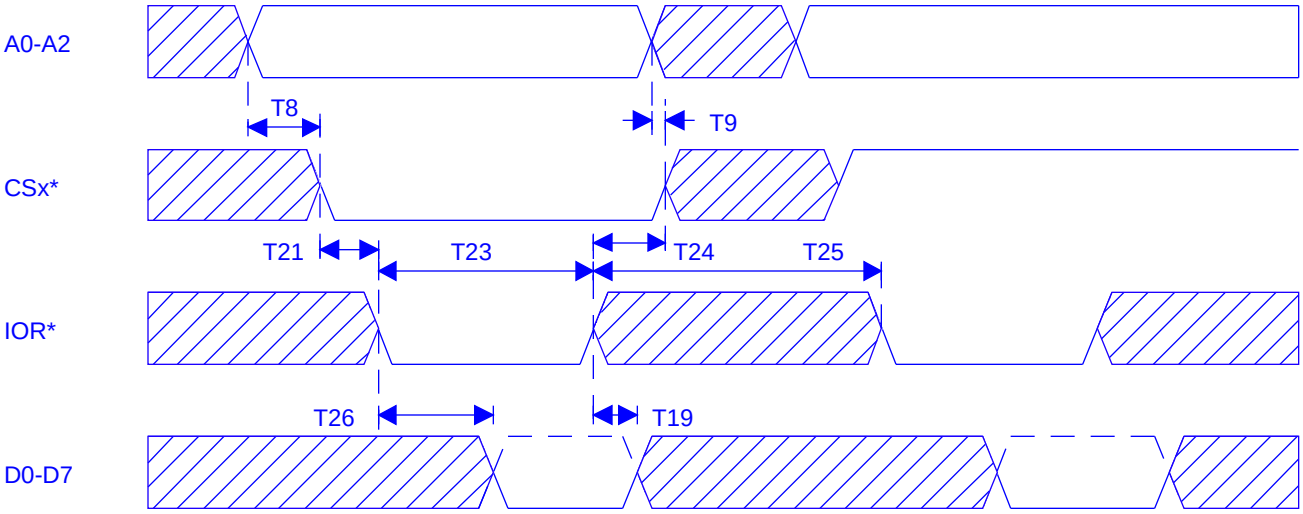
Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{ILCK}	Clock input low level	-0.5		0.6	V	
V_{IHCK}	Clock input high level	3.0		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		VCC	V	
V_{OL}	Output low level on all outputs			0.4	V	I_{OL}= 6 mA
V_{OH}	Output high level	2.4			V	I_{OH}= -6 mA
I_{CC}	Avg power supply current		5	7	mA	
V_{OP}	Operating voltage	3		5	V	
I_{SLP}	Avg sleep mode current		200	500	µA	
I_{IL}	Input leakage			±10	µA	
I_{CL}	Clock leakage			±10	µA	
R_{IN}	Internal pull-up resistance	5		15	kΩ	*Marked pins

CLOCK TIMING



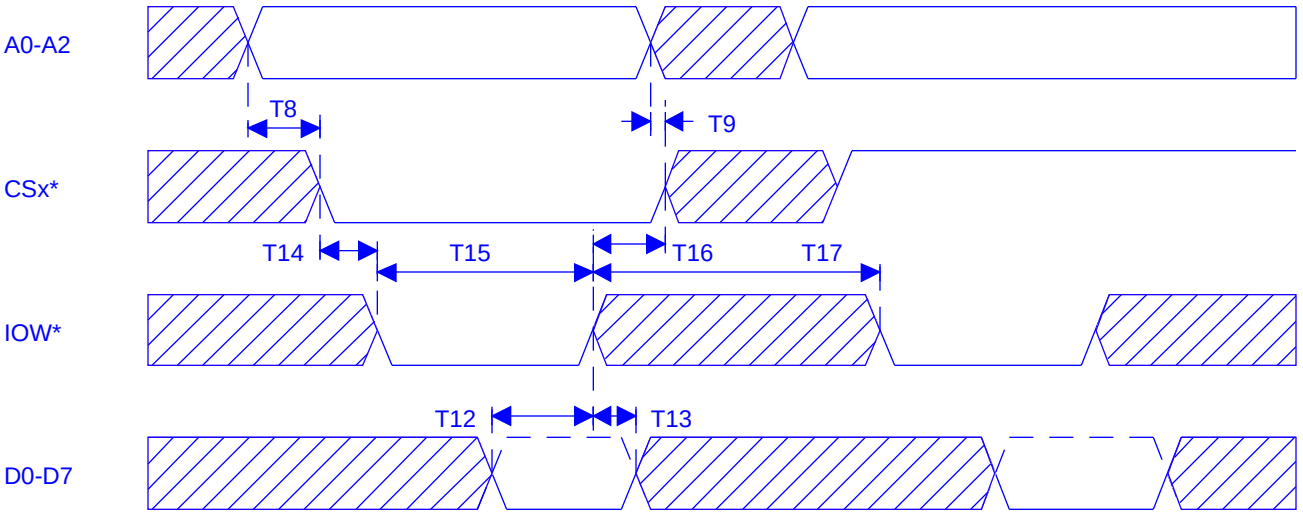
ST16C654

GENERAL READ TIMING



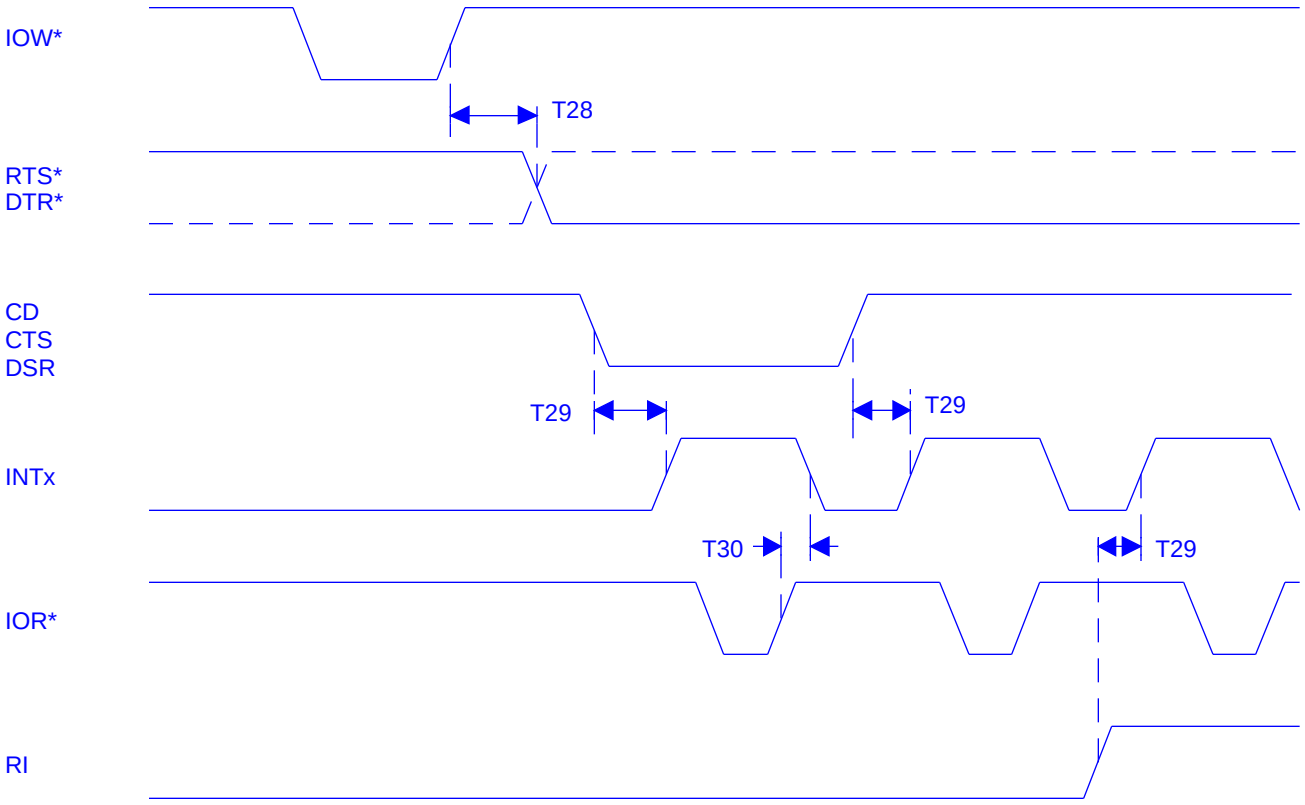
162450-RD-1

GENERAL WRITE TIMING



162450-WD-1

MODEM TIMING



162450-MD-1

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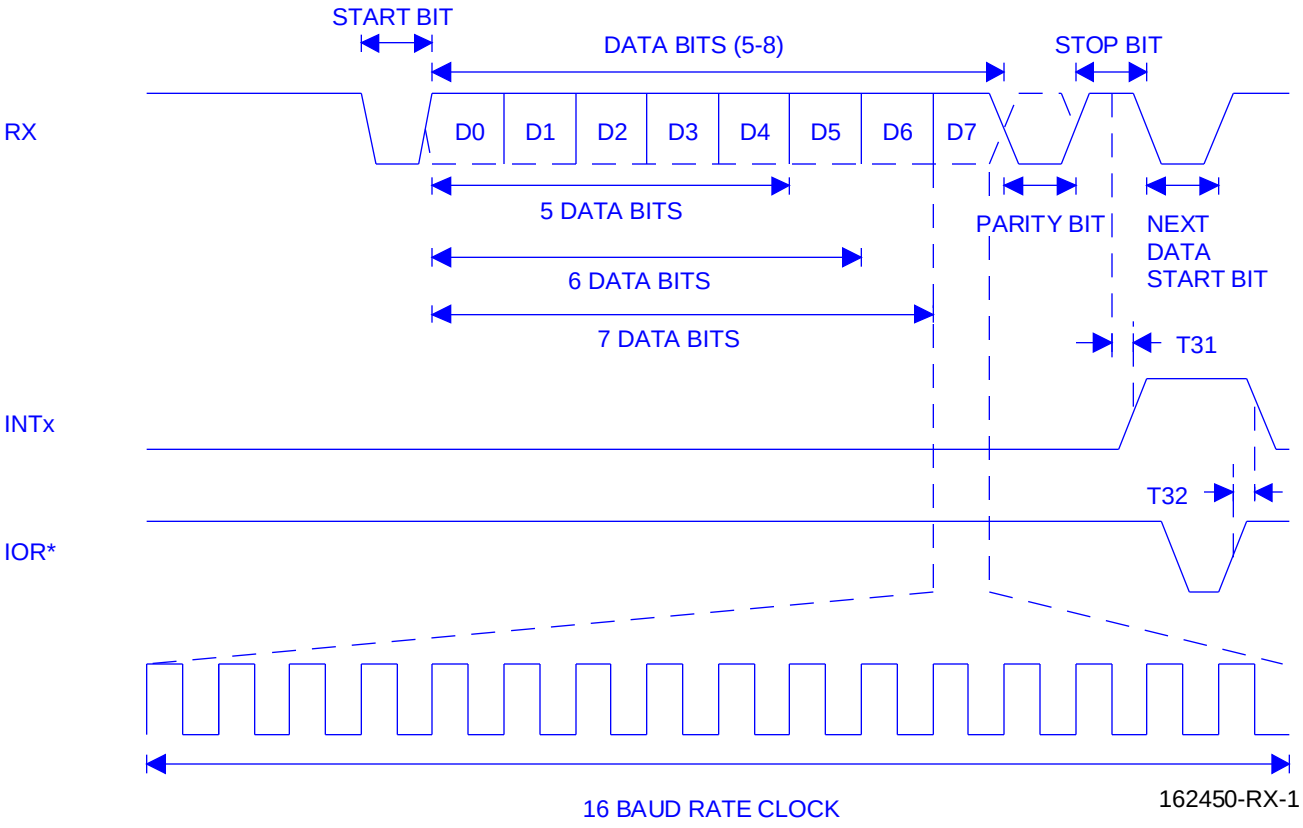
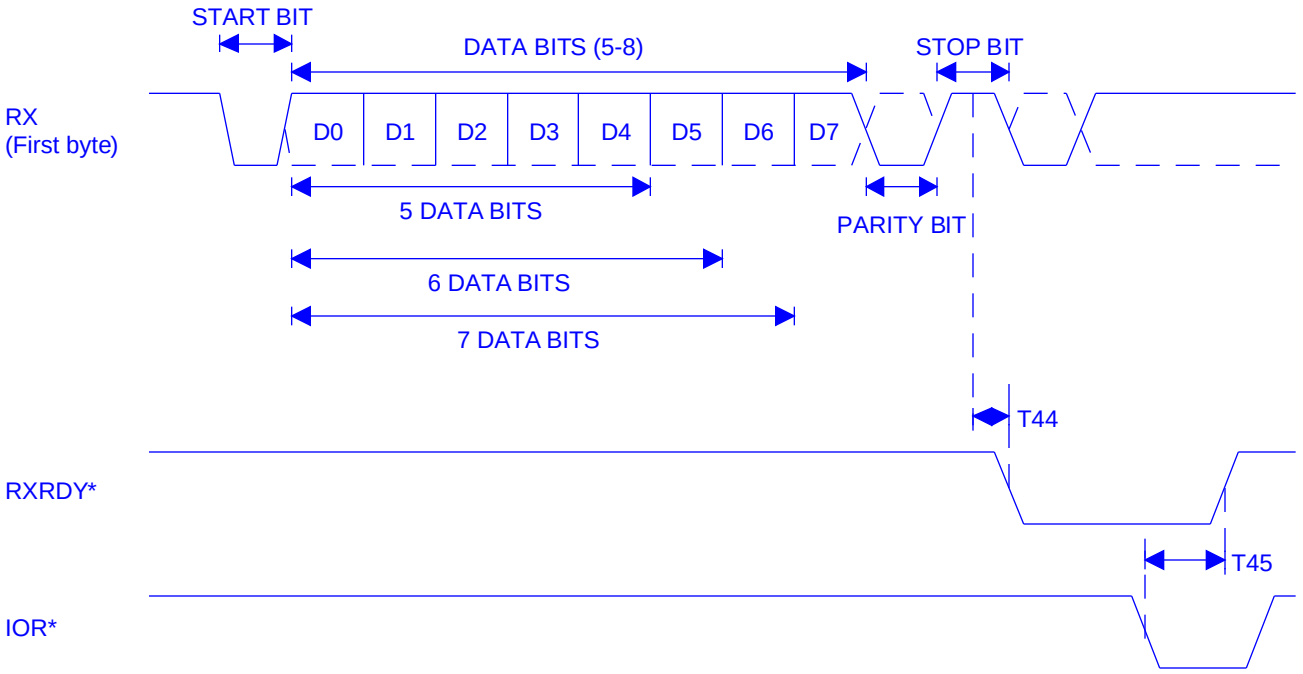
RECEIVE TIMING



RXRDY TIMING FOR MODE "0"



16552-RX-2

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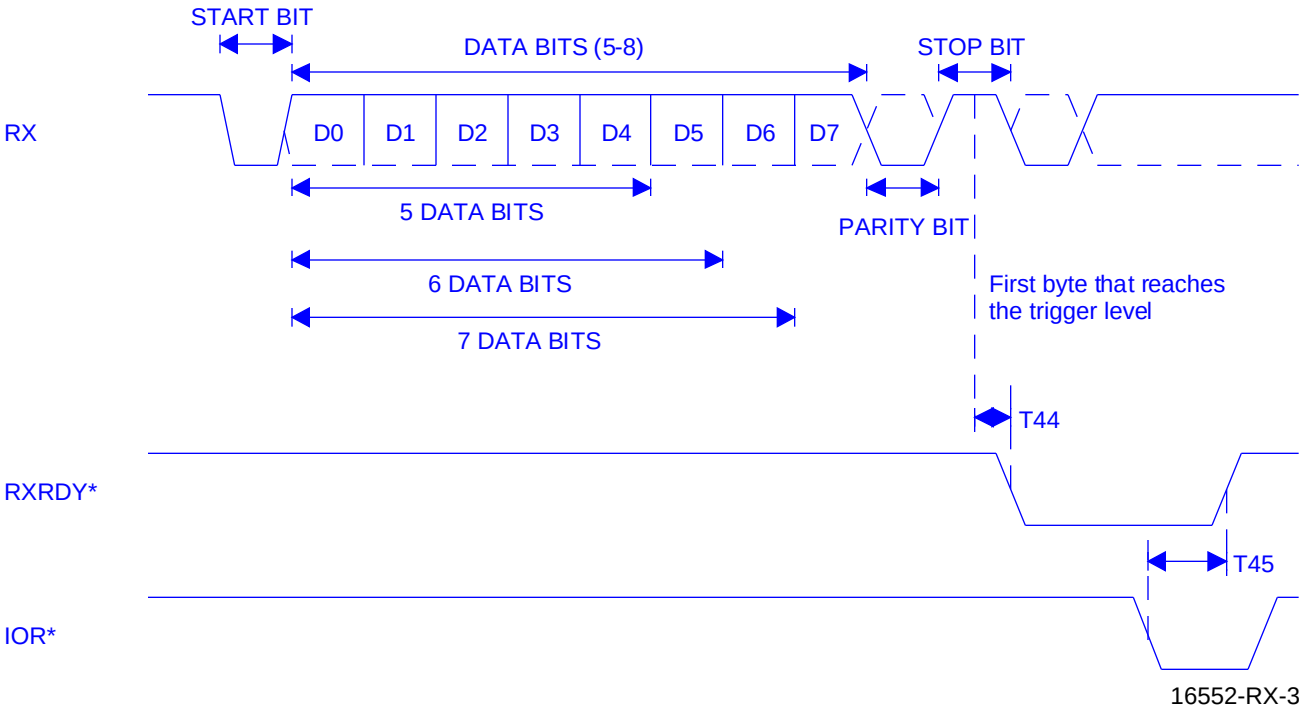
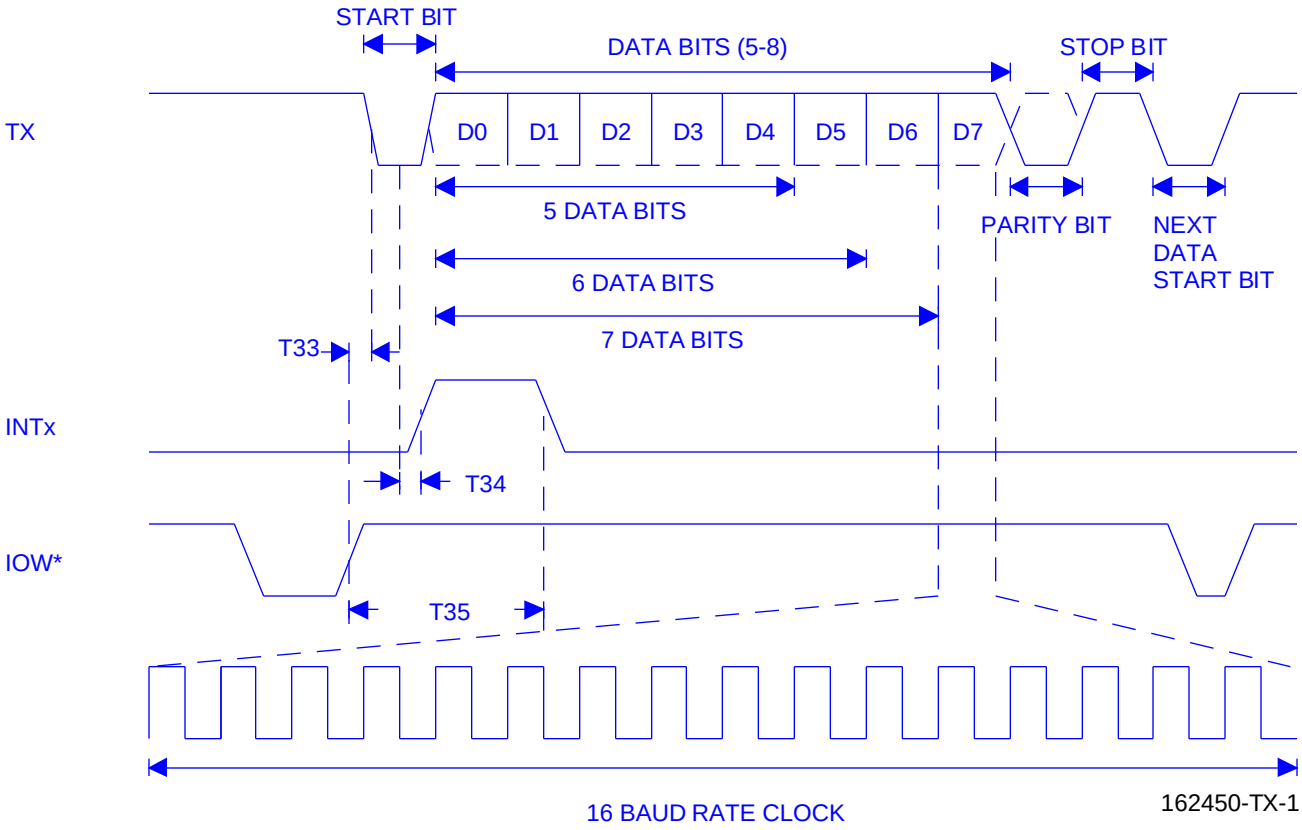
RXRDY TIMING FOR MODE "1"



ST16C654

TRANSMIT TIMING



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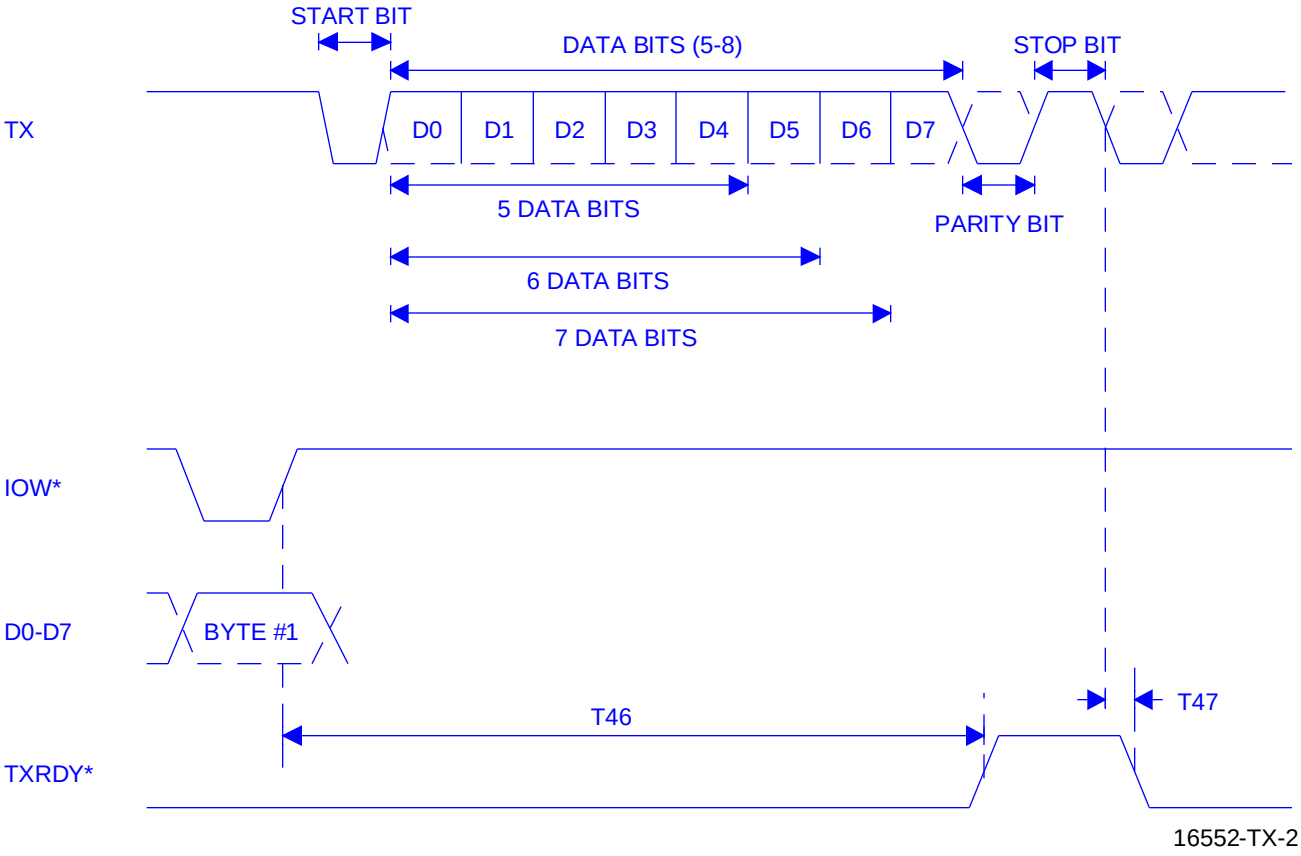
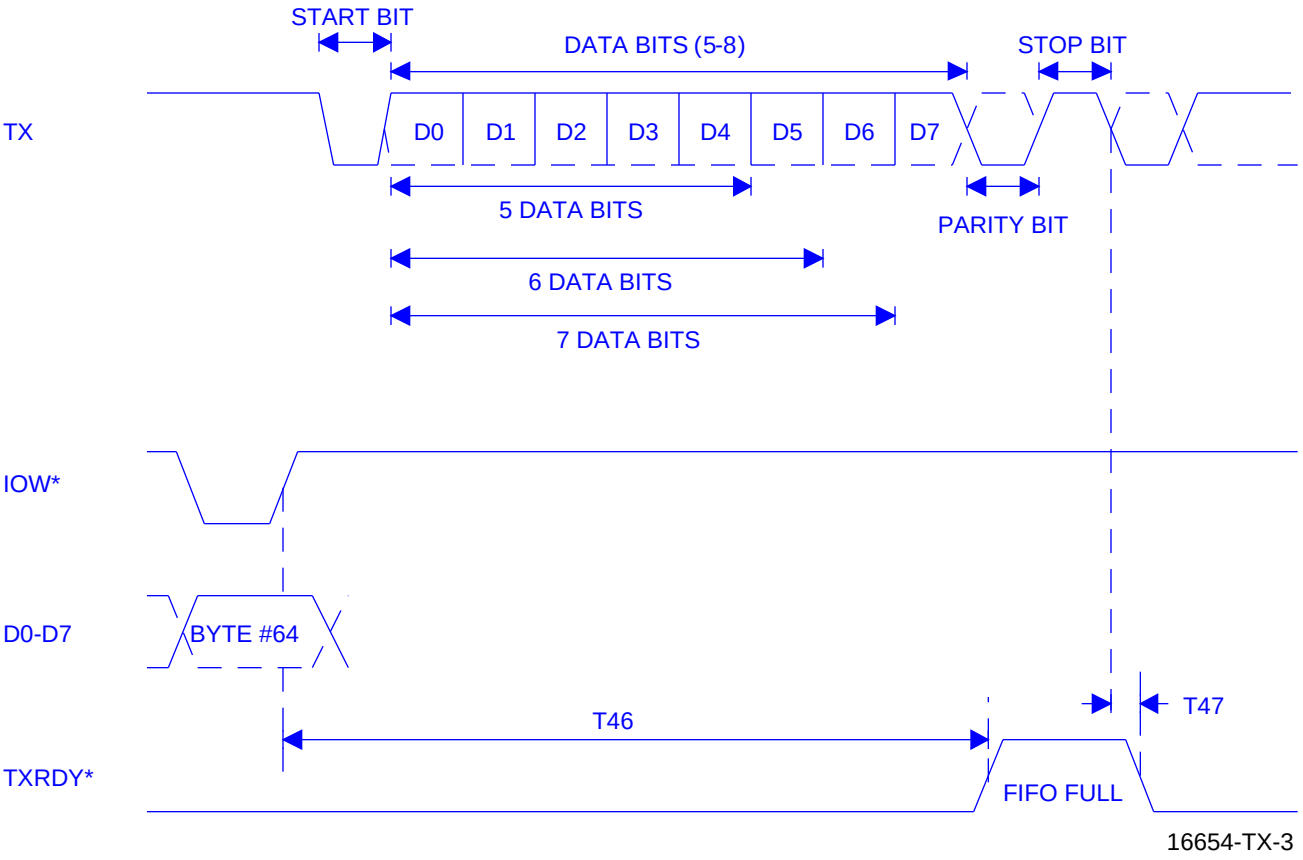
TXRDY TIMING FOR MODE "0"

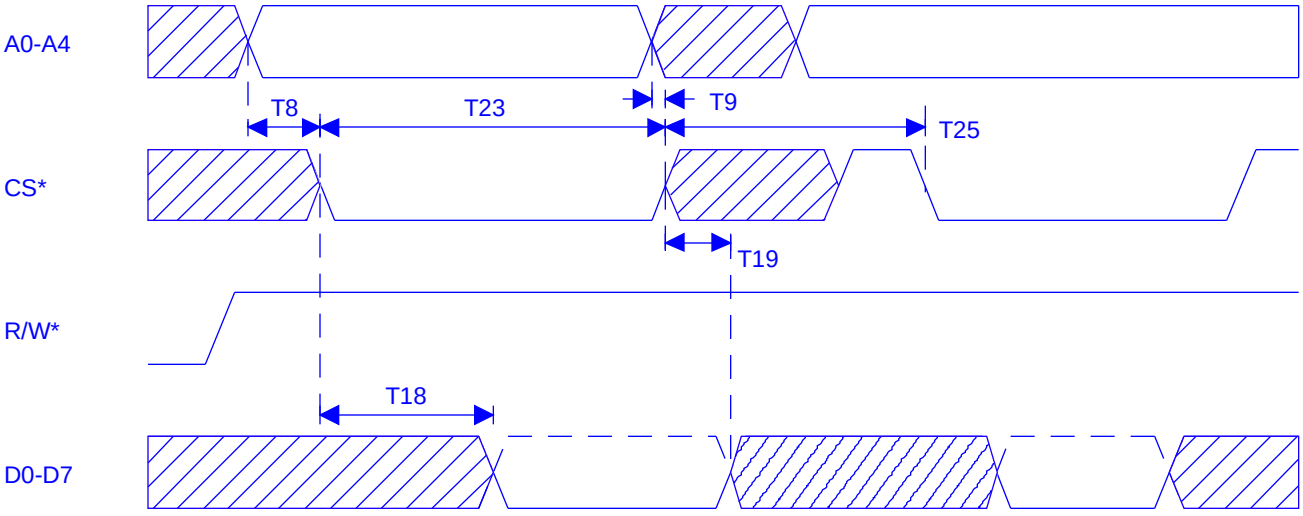


TXRDY TIMING FOR MODE "1"



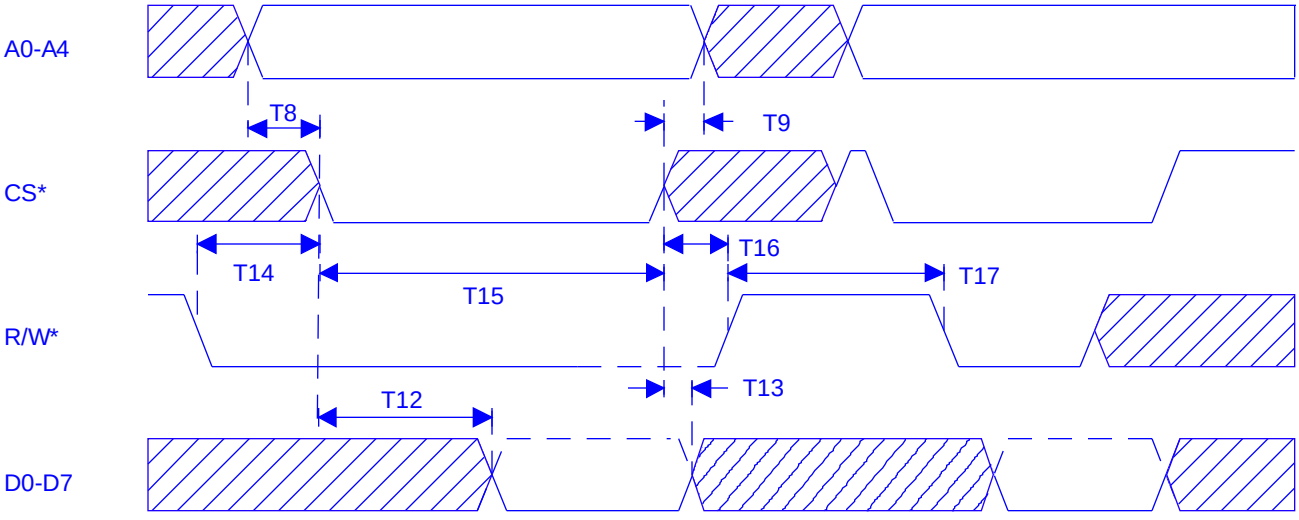
ST16C654

GENERAL READ TIMING



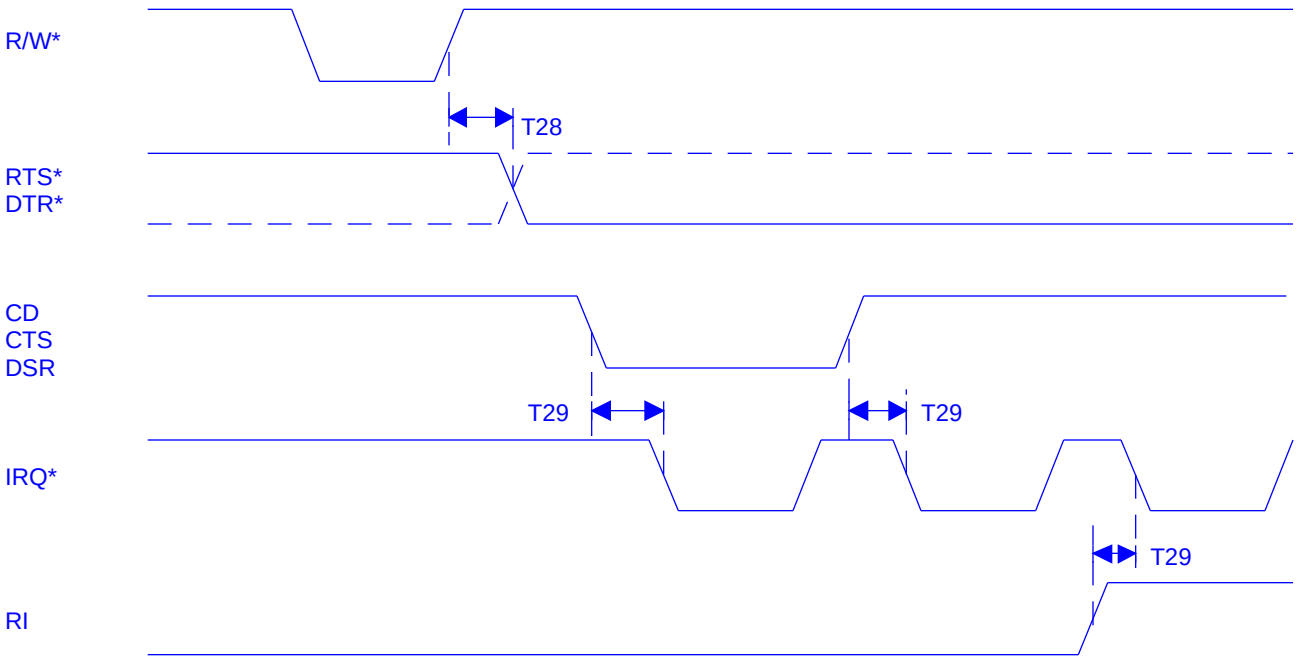
8454-RD-2

GENERAL WRITE TIMING



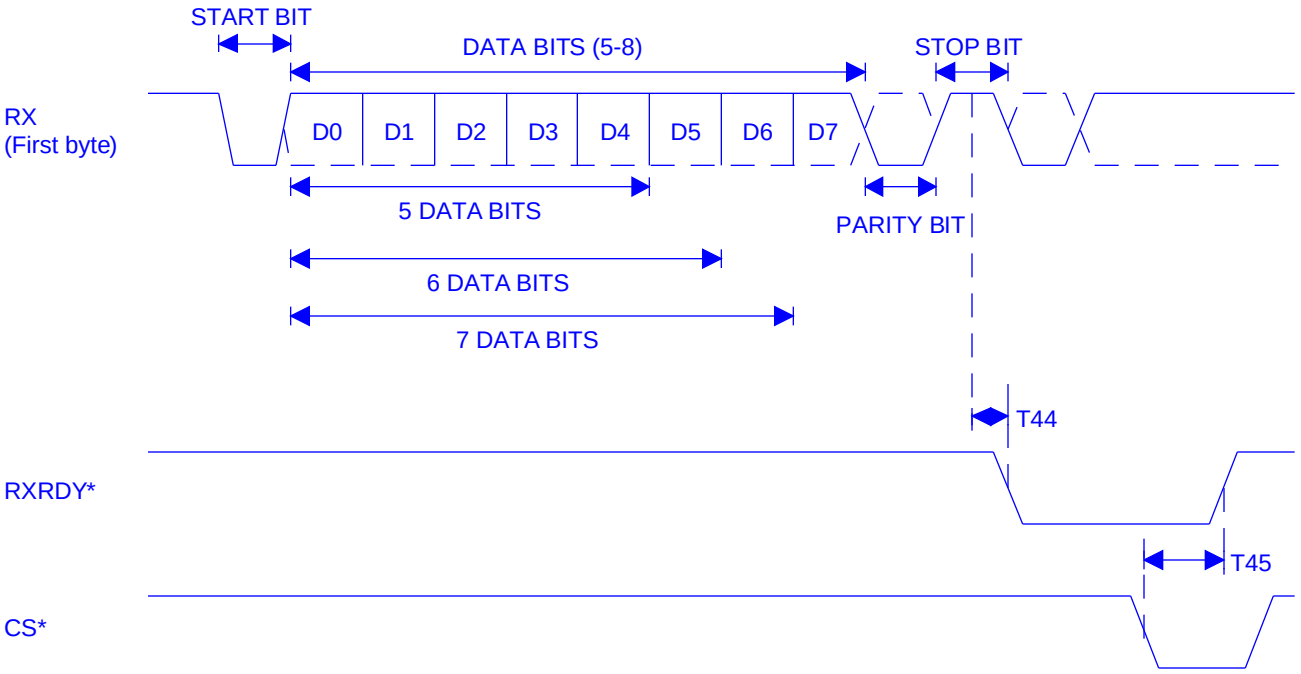
68454-WD-1

MODEM TIMING



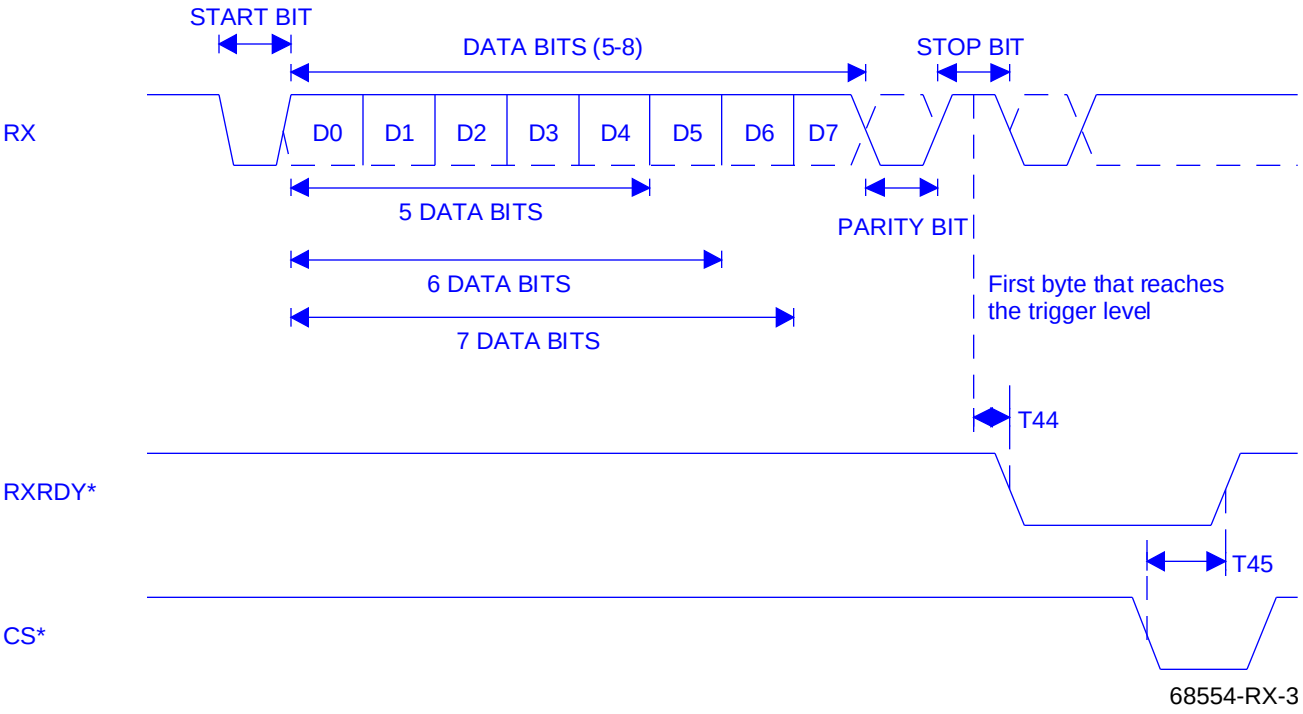
ST16C654

RXRDY TIMING FOR MODE "0"



68554-RX-2

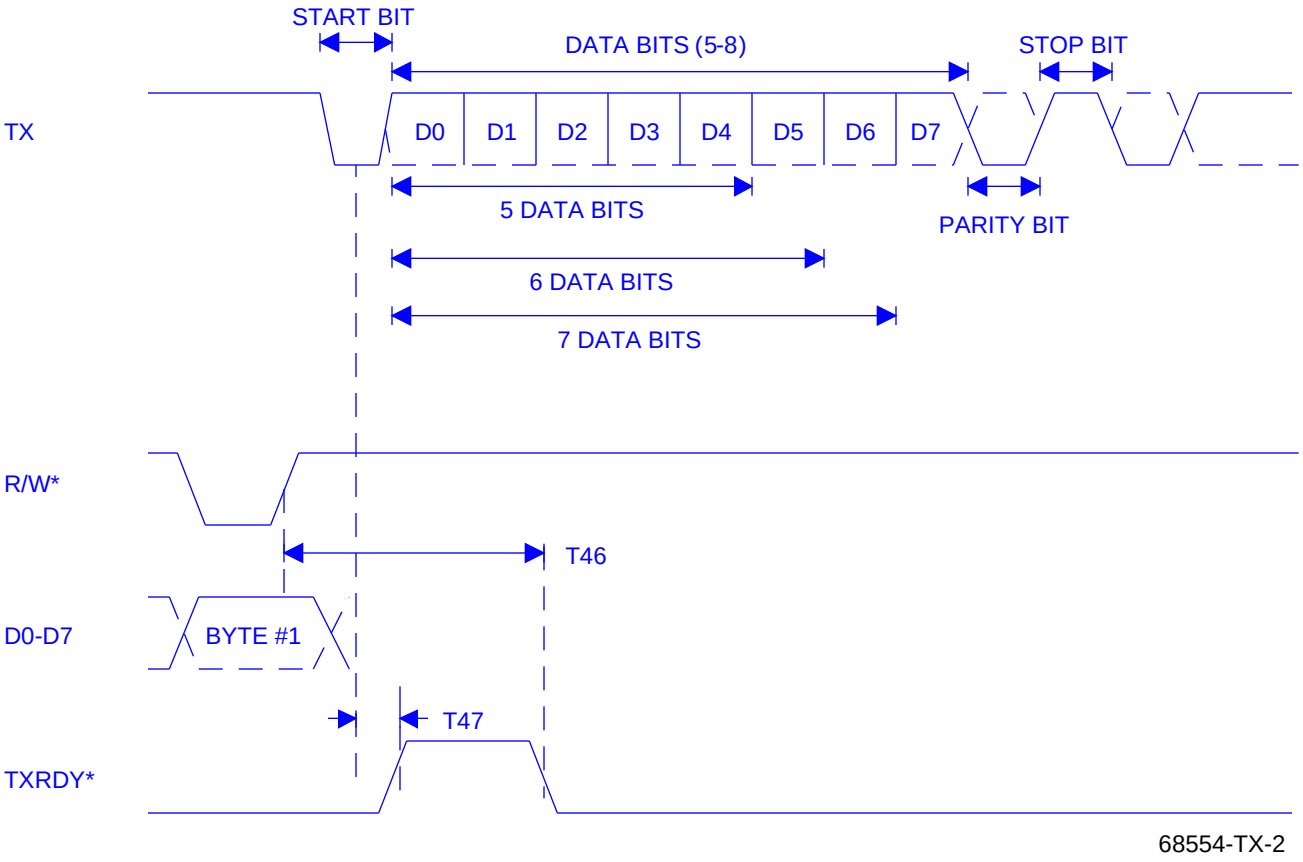
RXRDY TIMING FOR MODE "1"



Patent pending

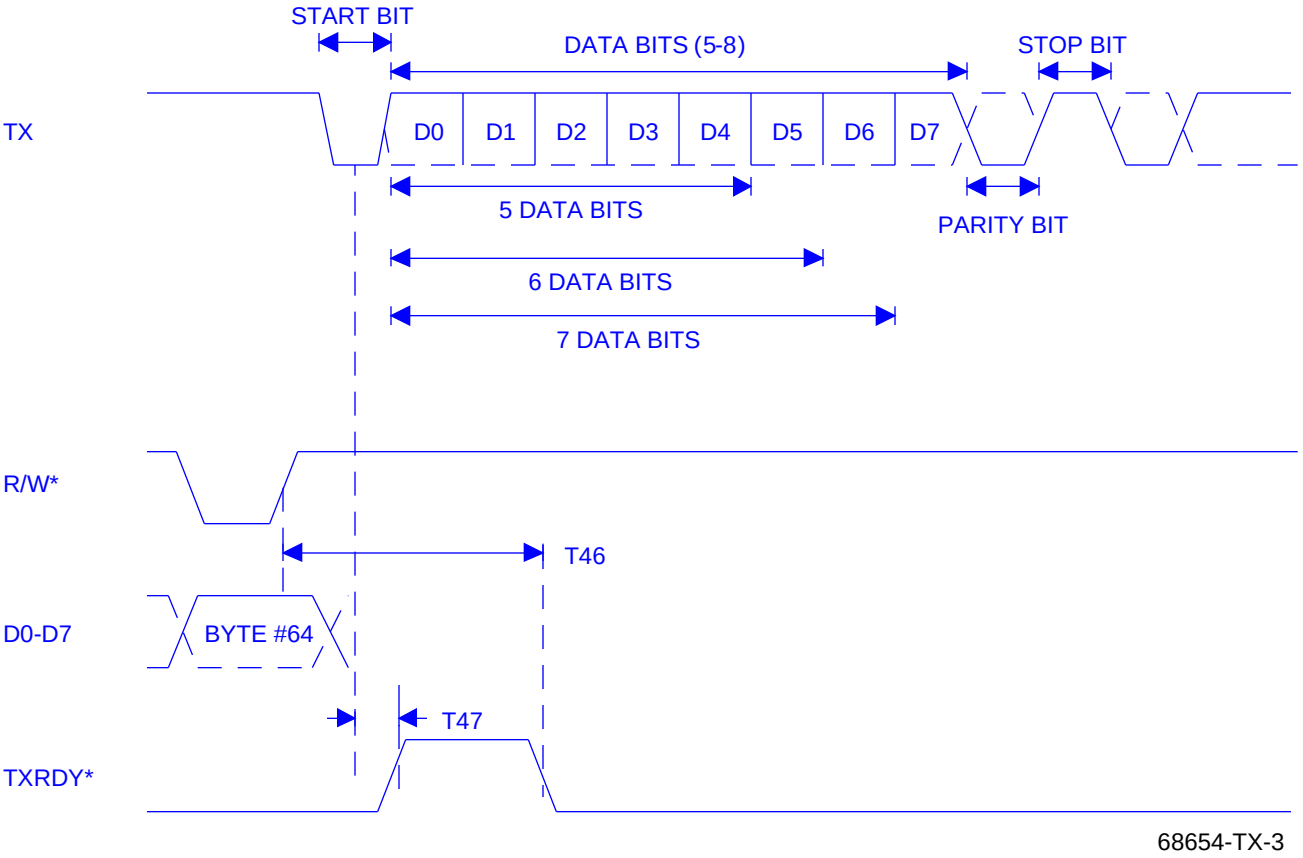
ST16C654

TXRDY TIMING FOR MODE "0"



68554-TX-2

TXRDY TIMING FOR MODE "1"



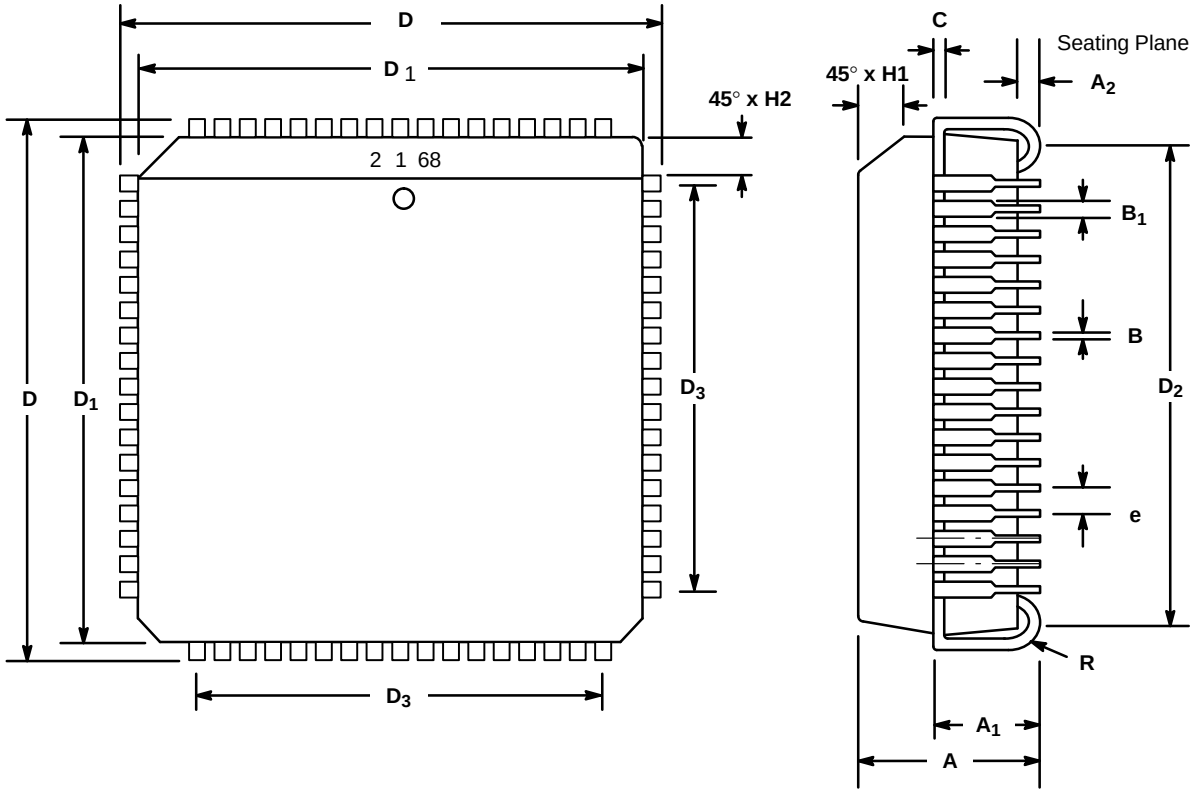
68654-TX-3

ST16C654

Package Dimensions

68 LEAD PLASTIC LEADED CHIP CARRIER (PLCC)

Rev. 1.00



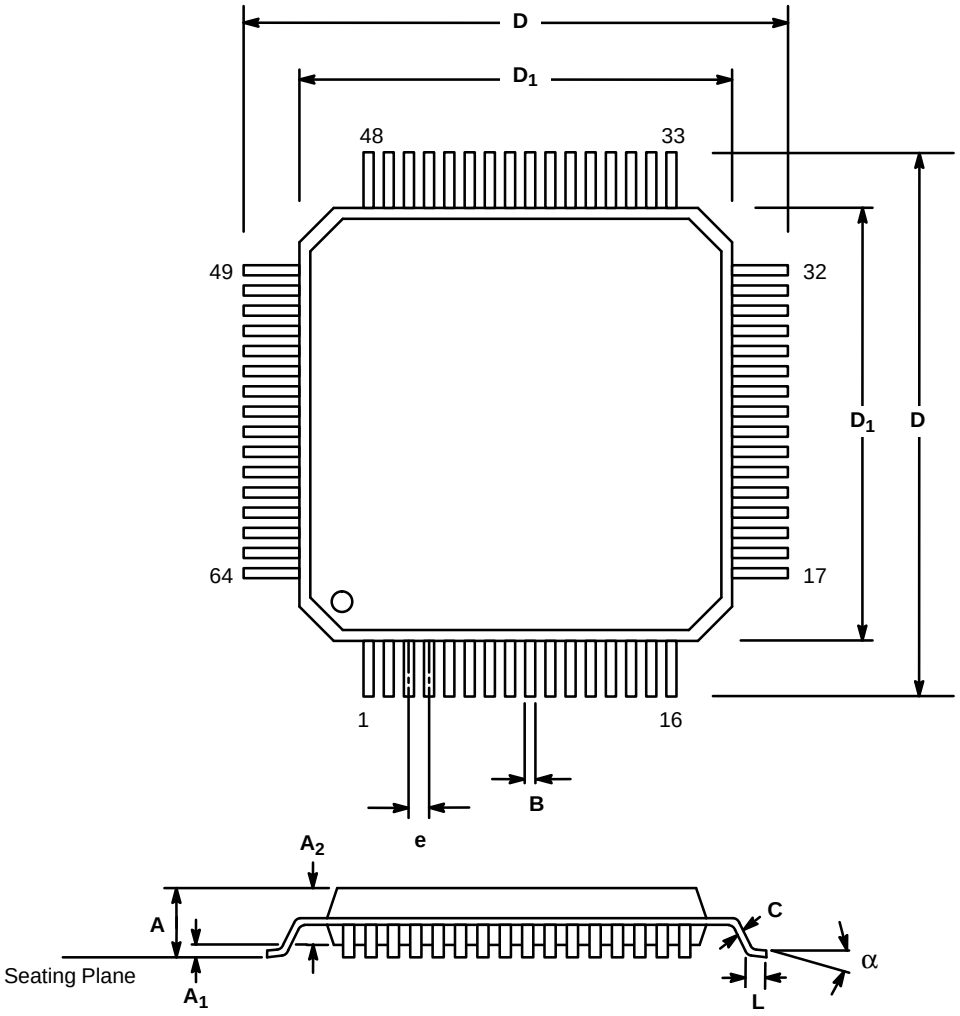
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.165	0.200	4.19	5.08
A_1	0.090	0.130	2.29	3.30
A_2	0.020	—.	0.51	—
B	0.013	0.021	0.33	0.53
B_1	0.026	0.032	0.66	0.81
C	0.008	0.013	0.19	0.32
D	0.985	0.995	25.02	25.27
D_1	0.950	0.958	24.13	24.33
D_2	0.890	0.930	22.61	23.62
D_3	0.800 typ.		20.32 typ.	
e	0.050 BSC		1.27 BSC	
H1	0.042	0.056	1.07	1.42
H2	0.042	0.048	1.07	1.22
R	0.025	0.045	0.64	1.14

Note: The control dimension is the inch column

Package Dimensions

64 LEAD PLASTIC QUAD FLAT PACK
(14 mm x 14 mm, QFP)

Rev. 1.00



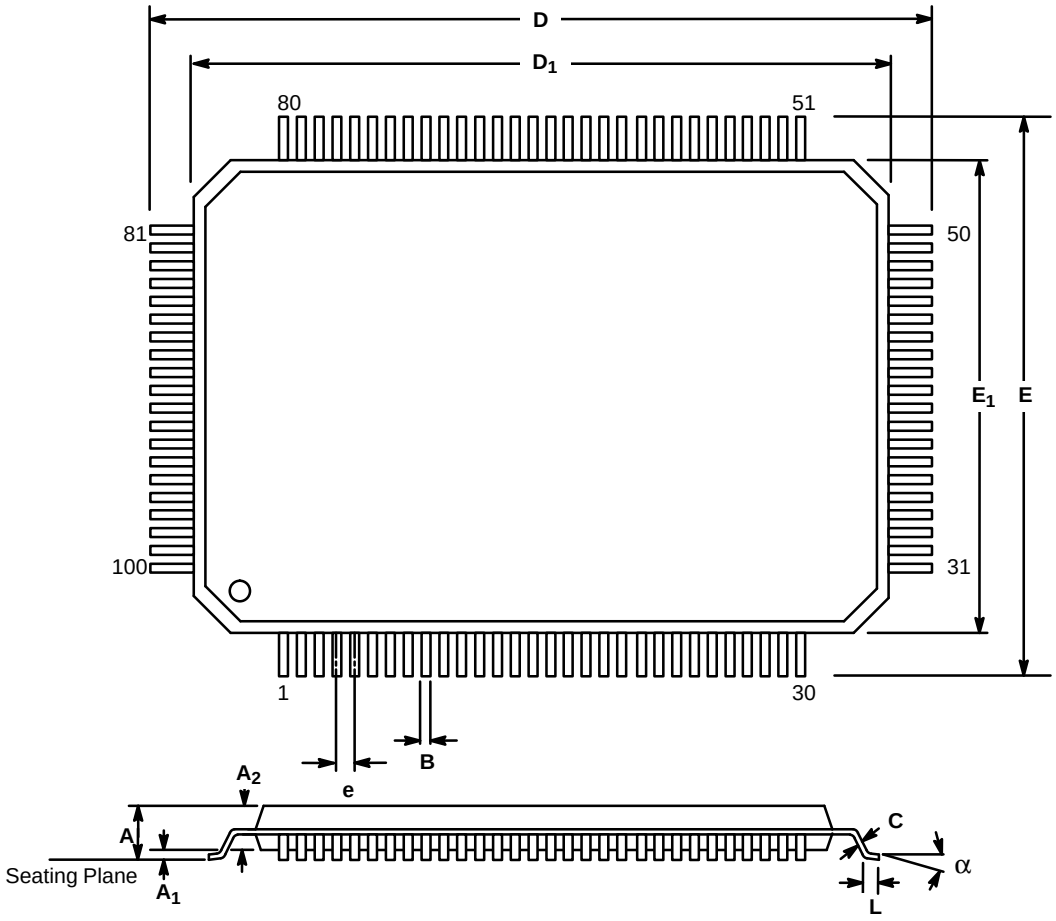
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.110	0.134	2.80	3.40
A_1	0.010	0.014	0.25	0.35
A_2	0.100	0.120	2.55	3.05
B	0.012	0.018	0.30	0.45
C	0.005	0.009	0.13	0.23
D	0.667	0.687	16.95	17.45
D_1	0.547	0.555	13.90	14.10
e	0.0315 BSC		0.80 BSC	
L	0.026	0.037	0.65	0.95
α	0°	7°	0°	7°

Note: The control dimension is the millimeter column

Package Dimensions

100 LEAD PLASTIC QUAD FLAT PACK
(14 mm x 20 mm, QFP)

Rev. 2.00



	1.6 mm Form				1.95 mm Form			
	INCHES		MILLIMETERS		INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	0.102	0.130	2.60	3.30	0.102	0.134	2.60	3.40
A_1	0.002	0.010	0.05	0.25	0.002	0.014	0.05	0.35
A_2	0.100	0.120	2.55	3.05	0.100	0.120	2.55	3.05
B	0.009	0.015	0.22	0.38	0.009	0.015	0.22	0.38
C	0.005	0.009	0.13	0.23	0.005	0.009	0.13	0.23
D	0.904	0.923	22.95	23.45	0.931	0.951	23.65	24.15
D_1	0.783	0.791	19.90	20.10	0.783	0.791	19.90	20.10
E	0.667	0.687	16.95	17.45	0.695	0.715	17.65	18.15
E_1	0.547	0.555	13.90	14.10	0.547	0.555	13.90	14.10
e	0.0256 BSC		0.65 BSC		0.0256 BSC		0.65 BSC	
L	0.029	0.040	0.73	1.03	0.026	0.037	0.65	0.95
α	0°	7°	0°	7°	0°	7°	0°	7°

Note: The control dimension is the millimeter column

Notes

Notes

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